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FINAL REPORT

ANALYSIS OF JITTER CHARACTERISTICS IN A PULSE STUFFING TDM NETWORK

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HARRIS CORPORATION Electronic Systems Division
P.O. Box 37, Melbourne, Florida 32901 305/727-4000

FINAL REPORT

ANALYSIS OF JITTER CHARACTERISTICS IN A PULSE STUFFING TDM NETWORK

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The purpose of this study and breadboard development program was to provide an understanding of the performance of networks which utilize equipment employing pulse stuffing synchronization. The study was divided into two phases. Phase I covered a) analytical investigations of jitter characteristics, b) recommended jitter specification formulation and c) development of a breadboard testbed. Phase II covered testbed evaluation and experimentation.

The Phase I study approach consisted of developing three tools to study the jitter problem: a) mathematical models, b) a software simulator and c) a →

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breadboard testbed. In Phase II RMS and peak-to-peak jitter data were collected and analyzed for various system design parameter inputs. The output data of the test and evaluation phase were compared with the analysis simulation results. Descriptions of the analysis tools, experiments, and results for both phases are included in this report.

FOREWORD

This report describes results of a Study performed for the Defense Communication Agency under the auspices of the Defense Communication Engineering Center under contract DCA-100-76-C-0072. Mr. Dave Smith has served as Project Engineer for the Center. The work was performed during the period August 1976 through June 1977, under the direction of Mr. Art Richard and Dr. Thomas G. Zogakis. This report was submitted by the authors in June 1977.

The authors wish to acknowledge the significant contributions to this program by Messrs. Dave Smith and Ken Kirk of DCEC, and Mr. Sam Boor, Dr. Bibb Cain, Messrs. Ron Ensley, Hank Eyster, Ron Huhn, Mike Luntz, Jim Proctor and Art Richard of Harris ESD. Special acknowledgments go to Mrs. Melodie Poe, who diligently finalized the manuscript, and Mr. Ralph Gilley who fabricated, checked out the hardware simulation and laboriously collected the test data.

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SECTION 1.0

INTRODUCTION

1.0 INTRODUCTION

The development of the digital Defense Communications System (DCS) presents many technical problems related to, but different from those of developing bandwidth efficient digital transmission equipments for operation in a synchronous system. The more immediate problems are those of transition to a digital system in an orderly manner through a series of cost-effective equipment upgrades and replacements which fulfill the near term performance requirements and are compatible with the ultimate system. One such problem is the first and second level multiplexing functions in a digital DCS network which is initially nonsynchronous.

This problem contains both technological and economic aspects with regard to the performance and cost trade-offs between utilization of existing equipments and development of new equipments. A key element in these trade considerations is the ability to understand with confidence the performance of networks which contain equipments employing pulse stuffing techniques.

In the process of amassing information about pulse stuffing networks, Defense Communications Agency (DCA) sponsored this effort to study Jitter Characteristics in a Pulse Stuffing TDM Network. The study consisted of a two phase effort. Phase one, covered three of the four tasks in the statement of work:

Task 1 - Analytical Investigation of Jitter Characteristics
Task 2 - Recommended Jitter Specification Formulation
Task 3 - Development of a Breadboard Testbed

Phase two covered the last task:

Task 4 - Breadboard In Plant Test and Evaluation

This report covers the study results elicited from both phase one and phase two.

In support of the analytical investigation (Task 1) a combined discrete event-continuous software simulation has also been developed. This simulation has greatly enhanced our time domain analysis approach in the formulation of jitter characteristics and has provided considerable direction for formulating experiments performed in Task 4. The overall study encompassed analysis, software simulation, and hardware simulation.

1.1 Study Objectives

The primary objective of this study was to provide knowledge of the performance of networks utilizing pulse stuffing equipment and to assist DCA in performing the above trade-offs by quantifying the performance of existing equipments and concepts through both analytical and empirical means. In order to better delineate the primary objective, it was partitioned into a series of specific objectives as follows:

- Characterize Pulse Stuffing Jitter

  This objective was to gain a thorough understanding of the mechanisms which create pulse stuffing and waiting time jitter and to develop quantitative techniques to express their characteristics.

- Characterize Existing Pulse Stuffing Multiplexers

  This objective provided a quantitative understanding of the performance of the existing T1-4000 and AN/GSC-24 second level multiplexers. It further provided an understanding of the strengths and weaknesses of the pulse stuffing jitter performance of these devices and a qualitative recommendation for possible improvements.

- Characterize Stuffing Jitter in Tandem Networks

  This objective provided an understanding of the network effects related to pulse stuffing jitter. This objective will characterize the jitter produced by n-tandemed pulse stuffing multiplexers in network configurations.

- Determine Stuffing Jitter Performance Effects

  This objective provided an understanding of the mechanisms by which first level multiplexer performance is degraded by pulse stuffing jitter. It also provided techniques to quantitatively express the performance degradation.

- Characterize Existing First Level Multiplexers

  This objective provided a quantitative understanding of performance of an existing first level multiplexer, TSEC/CY-104, as a function of input pulse stuffing jitter.

- Develop Specifications

  This objective provided specifications which allow procurement of new or upgrading of existing first and second level multiplexing equipment to provide performance of a known standard.

- Develop a Testbed

  This objective provided a method to enhance the theoretical analysis by providing an experimental facility with sufficient flexibility which could confirm the conceptual analysis and in turn force the analysis to look at practical hardware limitations and hardware introduced problems. In addition, it provided a realistic aspect to the task of jitter measurement required to verify specification compliance.

- Testbed Evaluation and Testing

  This objective consisted of an in-plant evaluation of the testbed implementation. It was also desired to determine jitter accumulation characteristics by collecting test data on the output of single and multiple multiplexer/demultiplexer simulator connections and to determine the performance of a bit timing recovery circuit in a tandem configuration.

The goal was to provide an understanding of limitations resulting from the use of existing equipments and specifications for critical parameters for new equipments such that satisfactory pulse stuffing jitter performance will be achieved in the transitional digital DCS.

1.2 Study Results

The study results which have evolved in the effort are perhaps better understood when presented under the specific study objectives. A brief description of results under each objective is presented herein.

- Characterization of Pulse Stuffing Jitter

  Pulse stuffing jitter was studied under the separate categories of stuffing jitter and waiting time jitter. Expressions have been derived to describe the effects separately in order to provide an understanding of each category's cause and effect. This is instrumental in establishing trade-offs for the smoothing loop design and the second level multiplexer functional approach.

- Characterization of Existing Pulse Stuffing Multiplexers

  Positive stuffing multiplexers (such as the Bell M12 and VICOM T1-4000) can be designed to operate in regions of overall lower pulse stuffing phase jitter, thereby, alleviating stringent requirements on the smoothing loop. (A more economical first order smoothing loop thus becomes a realistic candidate.) Positive-zero-negative multiplexers (such as the AN/GSC-24) which

don't have the additional degree of freedom of selecting the offset frequency range are forced to use more stringent smoothing loop filtering in order to achieve the same overall level of pulse stuffing phase jitter.

- Characterization of Stuffing Jitter in Tandem Networks

  Investigation of the effects of cascading second level multiplexers, using the software simulator MUXJIT, demonstrated that because of the controls designed into second level multiplexers RMS jitter does not necessarily increase as postulated in the literature. In addition, it is noted that care must be rendered during experimentation with fielded hardware to avoid systematic errors which can cause erroneous interpretation of results.

- Determination of Stuffing Jitter Performance Effects

  Basic expressions were derived concerning the trade-offs between narrow bandwidths required to maintain a high signal-to-noise ratio in the presence of spectrum noise and wide bandwidths required to track the incoming jittered signal and, consequently, reduce the signal-to-noise ratio because of timing errors.

- Developed Jitter Specifications

  Jitter slewing and cascading specifications were developed to MIL-STD-490 format and are included in Appendix A of this report.

- Developed a Breadboard Testbed

  A hardware simulator was designed and implemented during this phase. It provides three sets of jitter simulator and smoothing loop functions which simulate second level multiplexers. Documentation of this design is contained in a companion document, "Design Plan for Pulse Stuffing TDM Network Study." The study has shown the requirement for a special Jitter Test Set needed to obtain measurements of peak-to-peak phase jitter in the Second Level Multiplexer Simulator (SLMS) as well as fielded equipment. This is basically done by obtaining a plot of phase variation versus time.

- Breadboard Evaluation

  Jitter data were generated, collected and plotted for direct comparison with MUXJIT results. The hardware simulator jitter data compared favorably with the software simulation.

- Collection of Jitter Characteristics via Breadboard Experiments

  Jitter data were collected for simulated multiplexer/demultiplexer nodes in tandem. The results did not show any accumulation of jitter. Duttweiler type curves were produced which compare favorably with the theoretical curve.

- Characterization of Existing First Level Multiplexers

  Testing using the hardware simulator and the E-CDS Receive Unit of the HN-74 in the TSEC/CY-104 Interface Unit was performed during Phase II of this program to measure bit error rates.

1.3 Program Assumptions and Conditions

The following key ground rules and assumptions have been established to govern the conduct of technical activity during this study. These are necessary because a quick search of the literature reveals a certain inconsistency in terminology, and subsequent discussion can conceivably be misconstrued by a reader's misunderstanding of nomenclature.

1. The study was mainly involved with second level multiplexers. A second level multiplexer for the purpose of description is defined as one which receives and/or disperses sequential streams of digital data. Each stream is handled under control of its own independent clock whose rate is plesiochronous with the other rates in the same multiplexer. (Plesiochronous is defined as a signal which has the same nominal digit rate but not synchronized to other signals in the same system.) A first level multiplexer was consequently defined as one which receives and/or disperses data under control of one master clock. Data routed through a typically deployed system passes through a first level multiplexer, which collects voice, teletype, telemetry, etc., source data, a cascaded sequence of second level multiplexers/demultiplexers which permit routing and transportation of the data through the complex network maze to its destination, and a first level demultiplexer which delivers the data to its destination. A first level multiplexer was involved in this study only to the extent that it is the final recipient of the data handled by the second level multiplexers. It must be able to synchronize and track the data stream without data loss (bit slip). To clarify terminology, a multiplexer unit is defined to have the capability to handle both the multiplexing and demultiplexing functions.

2. The technique used by the second level multiplexers to synchronize the various plesiochronous data streams into a single time division multiplexed data stream was assumed to be pulse stuffing (justification). Pulse stuffing is defined as the process for changing the rate of a digital stream in a controlled manner so that it can accord with a rate different from its own inherent rate, normally, without loss of information.

3. The jitter effects considered in this study were those caused by using pulse stuffing techniques to attain data stream synchronization. More specifically, the jitter caused by removing the stuffed bit and using a smoothing loop which does not compensate perfectly for the jitter created in the data stream by the absence of that bit was the thesis of this investigation. Other effects such as (a) jitter caused by the uncertainty of extracting clock from bipolar or NRZ data without a companion timing signal and, (b) variations in data rates such as doppler effect (if the link is relayed via satellite), environmental influences, etc., while pertinent to the overall jitter problem were not considered within the scope or objectives of this study. The primary objectives were to study the effects of pulse stuffing on clock timing, which drives and imparts jitter to the data stream, to characterize this jitter effect, and to contribute techniques to specify and measure pulse stuffing jitter.

4. It was postulated that in applications of interest the output data stream from the first level multiplexer could be encrypted data. In order to recover the information transmitted, it is imperative that bit count integrity be preserved in the data stream transmission until the data reached the decrypting device in the first level demultiplexer. Other criteria such as the effect of jitter on voice channel performance were considered beyond the scope of the study. Initial calculations indicated that a moderate amount of jitter would not seriously degrade voice quality. It was also observed that criteria to determine acceptable/unacceptable voice degradation is difficult to attain since voice has to be degraded severely before it can be unintelligible. Consequently, bit count integrity was the criteria considered to determine acceptable/unacceptable jitter.

5. For the purpose of designing the hardware simulator, the output rate of the first level multiplexer was assumed that of a Bell T1 channel, 1.544 MHz. This restriction evolves from the impracticality of providing a selectable range of center frequencies for the smoothing loop's NCO (numerically controlled oscillator). However, this condition is not overly restrictive. The hardware simulation at this data rate, (a) promotes a representative insight to the jitter characteristics, (b) satisfies the requirements of verifying the software simulator and analysis results and, (c) provides the practical hardware depth to the problem which is often lacking in the pure analysis and software simulation approaches.

1.4 Report Organization

This report is directed primarily at the analysis, recommended jitter specification and test and evaluation tasks, which are Task 1, Task 2, and Task 4, respectively. Task 3 is the Second Level Multiplexer Testbed development. This breadboard testbed development to simulate second level multiplexers has been discussed in detail in the "Design Plan for Pulse Stuffing TDM Network Study," which was submitted earlier.

Section 2 discusses in depth the overall study approach. This section is necessary to understand the relevance of the other report sections.

Section 3 discusses basic definitions necessary for the study and an overall model of the operation of a pulse stuffing multiplexer. In addition, it discusses the pertinent state of the art data for existing and proposed multiplexers. This information was obtained from a perusal of the literature, device specifications, and maintenance manuals. Information obtained and documented in Section 3 is useful in setting the stage for the analysis approach.

The mathematical models, computer simulation, and the hardware simulator are described in Section 4. In essence, the approach taken to analyze the pulse stuffing TDM phase jitter is covered in the description of these three tools.

The results of these tools are discussed in Section 5. The basic effects of stuffing ratio, smoothing loop parameters, and cascaded nodes on both stuffing jitter and waiting time jitter are discussed. In addition, trade-offs involved in selecting a second level multiplexer, a smoothing loop and the first level multiplexer bit synchronizer are discussed. These trade-offs include jitter characteristic impact on first level multiplexer and other design criteria.

In Section 6.0 the results of the test and evaluation phase are discussed. This includes a description of the test matrix, laboratory test configuration, and a qualitative analysis of the individual experiments that were performed.

The last section, Section 7, contains the major conclusions and recommendations of the study. This effort has uncovered several areas for future investigation which encompass both additional analysis and hardware development.

SECTION 2.0

STUDY APPROACH

2.0 STUDY APPROACH

This study is structured around the requirements of the SOW. It is a two phase effort with the first phase covering (1) analysis, (2) jitter specifications and (3) breadboard test bed development. The fourth and last task, test bed operational verification and jitter evaluation, is Phase II.

In the classical study epoch, the analysis task has served as the Definition Period, the jitter specification and test bed development acted as the Design and Development Period and the test bed study results verification served as an Operational Evaluation Period.

Figure 2.0, Study Organization, outlines the flow of the study and its interrelationships. The key element which has to be highlighted is the interrelationship of the analysis, software simulator, and hardware simulator. This interrelationship is briefly outlined in Table 2.0, Interrelationship of the Study Tools.

2.1 Approach to Phases I and II

There were three specific tasks that had to be accomplished under Phase I. Task 1 was an analysis task that was concerned with identifying and analytically evaluating the various types of jitter that can occur in pulse stuffing TDM networks. Its primary concern was with the analysis and characterization of jitter which resides on the output of a demultiplexer as a result of the inability of a smoothing loop to completely compensate for the removal of stuff bits. In addition, other types of jitter that can occur were identified, i.e., waiting time jitter, control bit extraction from the data stream jitter, and jitter generated from component instability.

Task 1 analyses were performed employing mathematical models and computer simulations. Extensive time and effort were expended in literature searches and document reviews. This information was incorporated into the models and simulations of Task 1.

Task 2 was concerned with the recommendation of jitter specifications for DCS multiplex equipment. These recommendations emerged from the results of the analysis performed under Task 1 and have been reinforced by the results of Task 4. Key performance parameters and methods of testing the specifications are defined where practical. There are cases where jitter

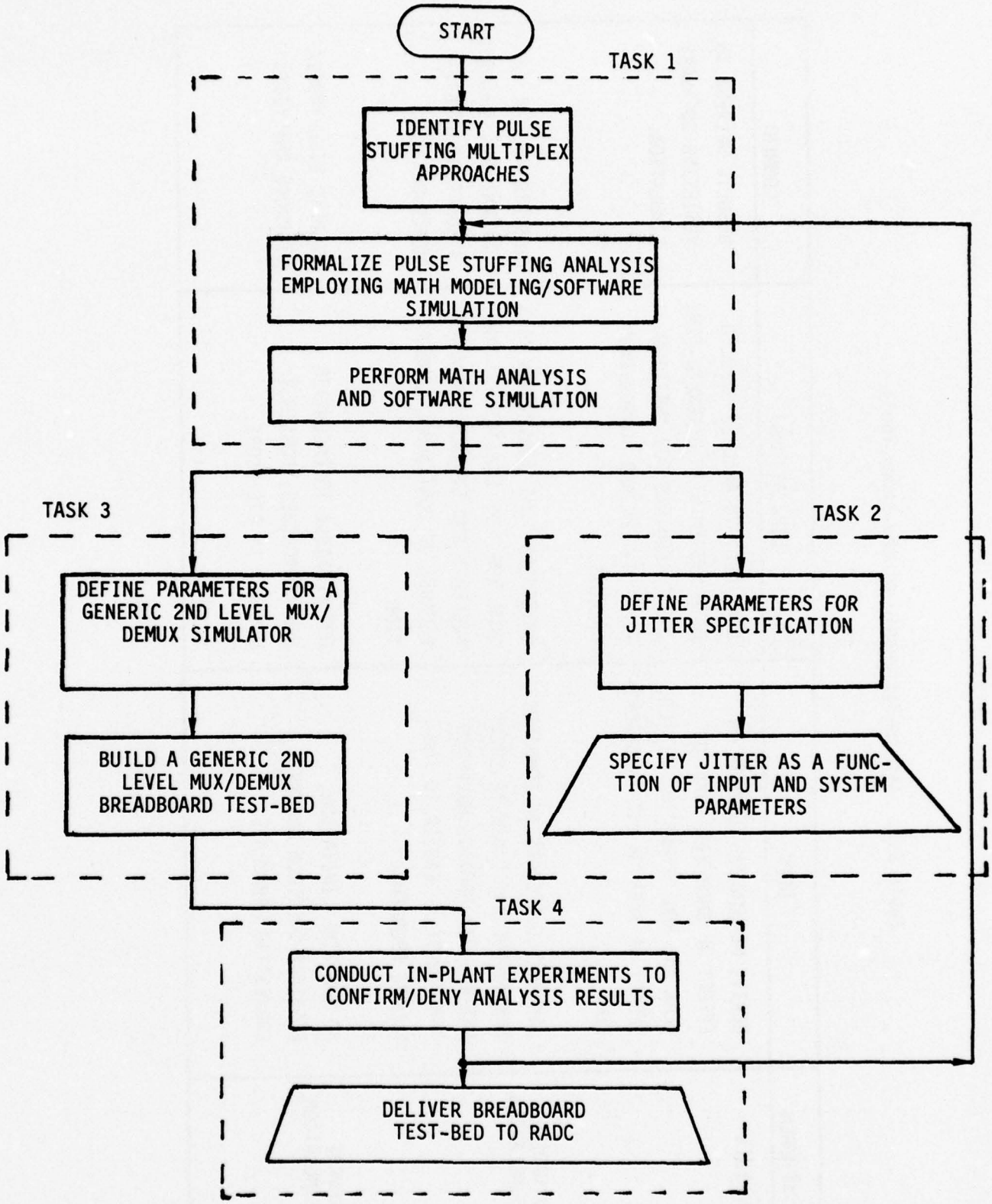


Figure 2.0. Study Organization

Table 2.0. Interrelationship of the Study Tools

APPROACH	USES	LIMITATIONS	COMMENT
ANALYSIS	DERIVE MEANINGFUL RESULTS ON EFFECT OF SMOOTHING LOOP ON PEAK AND RMS "STUFFING" JITTER, IMPACT OF SUCH ON BIT SYNCHRONIZER.	DIFFICULT TO ANALYZE SAMPLED-DATA SYSTEM WITH DISCRETE-TIME INPUT REQUIRED FOR "WAITING-TIME" JITTER AND "CASCADING" EFFECTS.	RESULTS HELPFUL IN VERIFYING SOFTWARE SIMULATION.
SOFTWARE SIMULATION	CAN HANDLE EFFECTS OF COMBINED CONTINUOUS AND DISCRETE-EVENT SYSTEM, CAN PROVIDE WAVEFORM "SNAPSHOTS." EASIER TO FORMULATE PROBLEMS.	BASICALLY TIME DOMAIN ANALYSIS SOME RUN TIME LIMITATIONS FOR ACCURACY AND STARTUP-TRANSIENT BECAUSE OF CONTINUOUS SIMULATION.	RESULTS HELPFUL IN DETERMINING HARDWARE SIMULATION EXPERIMENTS DESIRED.
HARDWARE SIMULATION	NO RUN TIME LIMITATION, POSSIBLE SPECTRUM ANALYSIS, EASIEST TO FORMULATE.	NOT FLEXIBLE TO ENCOMPASS NEW APPROACHES, POSSIBLY LIMITED IN ITS SCOPE.	RESULTS WILL PROVE/ DISPROVE ANALYSIS.

specifications are recommended which involve special test equipment or an extensive instrumentation equipment development program. They have been noted for future consideration assuming the development of more sophisticated jitter measuring equipment.

Task 3 is a breadboard testbed development. A testbed was developed using breadboard circuitry. Critical parameters which have been identified via Task 1, can be varied to study jitter in single node and multinode configurations. Three jitter simulators and their corresponding smoothing loops were incorporated on the breadboard. The breadboard circuitry has been constructed using standard rack mounted hardware to facilitate its delivery. The implementation of this testbed has been described in a design plan which was submitted to DCA for review and approval. This design plan contains a comparative discussion of candidate techniques, a recommended approach and a paper design of the recommended testbed. The testbed generates an equivalent Bell T1 1.544 Mbps PCM signal and, in addition, provides the capability to tandem a number of stuff/destuff and smoothing operations on the signal to verify the method in which jitter accumulates.

Phase II, Task 4, represents an in-plant test and evaluation phase for the testbed developed in Task 3. A test matrix was generated and incorporated in a test plan, *Test Plan for Analysis of Jitter Characteristics in a Pulse Stuffing* TDM Network, which was approved by DCA. This test matrix, along with a description of the tests, is reported in this document. The test plan contains the detailed test procedures for each experiment. This included the procedure for testing bit error rates of the E-CDS Receive Unit of the HN-74 from the CY-104 first level multiplexer when stimulated by a jittered waveform from the testbed. In Task 4 jitter data were collected for various parameter changes. Parameters which were varied were the tributary input data stream, the output data transport stream, number of bits per stuffing opportunity, and the filter bandwidth. These data have reinforced the conclusions that were generated during Task 1 and have closed the loop depicted in Figure 2.0 for this study.

There is a high degree of interaction and adaptive feedback between the various tasks of this study. An overview of the relationship of the various tasks in this study is shown in Figure 2.0. Note that Task 1 is the driving influence on the other tasks. It, however, is adaptable to the results of the other tasks. For example, Task 1 provides information from research and analysis to formulate jitter specifications. Because a desirable specification is not well defined, this prompts more analysis. This same situation arises with

Task 3. Because of scaling, parameter range determination, and stability requirements, which are more fully identified during a design, a need arose for additional analysis. Many of these circumstances arose during component selection and are attributable to the limitations on components and hardware design.

Since a major portion of this study was involved in the analysis task, it is appropriate to describe the approach. First, a literature search was undertaken to identify state of the art approaches and to identify existing pertinent first level and second level multiplexer parameters. Existing commercial practices and the applicable recommendations of CCITT, Special Study Group D, were perused. These ideas and data were used to generate mathematical models of peak-to-peak and RMS jitter in pulse stuffing networks. The effect of a smoothing loop on peak-to-peak and RMS stuffing jitter and the impact on a bit synchronizer for a single node were obtained. However, several limitations occurred for the mathematical models. It is difficult to analyze sampled data systems with varying discrete time inputs. Such analysis was needed to characterize waiting time jitter and multinode effects. Therefore, a software simulation had to be constructed. A simulation using GASP IV was generated to obtain a solution for the waiting time jitter and cascading effects in the time domain. The results from the math model for a single node were useful in checking out the program.

The software simulation can handle the effects of a combined continuous and discrete event system, provide easy to analyze waveform "snapshots," and conveniently output more statistical data in report form. The simulation is a time domain analysis, and this implies run time limitations for accuracy and startup transient. However, the results of the simulation were useful in determining parameters for the hardware development and recommended jitter specifications for system performance.

For Task 3 hardware jitter simulator/smoothing loop development, the decision to design a digital phase locked loop was based on the following factors:

- The ease of varying the system parameters over the ranges determined by the Task 1 analysis.
- Obtaining the maximum hardware and experimental flexibility with minimum cost.
- Flexibility in making modifications and additions to the hardware.

It is felt these factors provide the basis for a versatile, flexible, and cost effective testbed. This testbed is useful for evaluating existing multiplexer designs, jitter characteristics and accumulation, confirming or denying analytical results and simulations.

2.2 Objectives of Phase I

The overall study objectives were further divided so each task had its own set of objectives. Because of their top-down origin, the individual objectives are not divorced from each other. As stated previously, the primary goals of this study were to provide knowledge of the performance of networks utilizing pulse stuffing equipment and to assist DCA in gaining insight for performing the trade-offs necessary to choose existing equipments and concepts for future defense networks. This study utilizes both analytical and empirical approaches to obtain these objectives.

Task 1, which is an analytical investigation, is, in general, directed to modeling and analyzing the jitter created in second level multiplexers. To be more specific, Task 1 can be segmented into three subtasks. The objectives of subtask 1 are the following:

- Perform a literature search to identify existing practices and obtain pertinent data for first and second level multiplexers.
- Model generic pulse stuffing in single and tandem configurations for both positive and negative stuffing.
- Calculate phase jitter at the output of generic pulse stuffing in single and tandem configurations. This is essentially to quantify and analyze the characteristics of jitter accumulation in tandem multiplexer/demultiplexer connections.
- Study the effect of frequency offset (up to ±200 bps) for the nominal 1.544 Mbps asynchronous source on creation of jitter.
- Generate guidelines for judiciously choosing stuffing ratios.
- Apply analytical models to the specific cases of the VICOM T1-4000, Bell M12, and AN/GSC-24 to obtain information on the characteristics of jitter.

The objectives of subtask 2 are the following:

- Study the characteristics of first level demultiplexers with attention focused on the TSEC/CY-104 bit timing synchronizer.
- Obtain a model for a first level bit synchronizer.

- Determine the effect of jittered waveforms on this phase-locked loop of the timing recovery circuit to obtain insight into the mechanics of bit slip, acquisition frequency range, and time to acquire.

The objectives of subtask 3 are directed toward providing information and direction for the other Tasks in the study. The following objectives fall under subtask 3:

- From the analysis performed in subtask 1, provide information to recommend jitter specifications for DCS multiplex equipment.
- Employing the models in subtask 1, determine the parametric values necessary to design and implement the jitter simulators and smoothing loops in Task 3.

From the discussion above, it is tacit that the results of Task 1 are needed for incorporation in the other tasks. This is particularly true for Task 2. The objectives of Task 2 are the following:

- From the inputs provided by Task 1, recommend the maximum jitter allowed on second level demultiplexer outputs, maximum jitter which the first level multiplexer can accept, characteristics of jitter accumulation with tandem multiplex/demuliplex pairs, and maximum number of tandem multiplex connections allowed before the first level demultiplexer input interface requirements is exceeded.

- Word the specifications such that they will be based largely on industry standards and terminology (MIL-STD-490).
- Establish acceptance criteria for the equipment which are readily measurable in quantitative terms where possible.
- Point out specifications that are desirable, but the instrumentation equipment to measure acceptance criteria in quantitative terms has to be developed.

The final task in Phase I is the development of a breadboard testbed. The objectives of Task 3 can be characterized as follows:

- Design and implement jitter simulator/smoothing loop pairs with sufficient provisions for varying critical parameters to determine optimum performance.
- Implement the testbed facility so that it is conducive to verifying the analytical results of Task 1.

- Construct the breadboard circuitry sufficiently rugged to allow its delivery to the Government, subsequent to Phase II of this Study, In-Plant Test and Evaluation, for additional testing at RADC.
- The testbed shall use a typical equivalent 1.544 Mbps PCM signal.

2.3 Objectives of Phase II

Phase II was composed of a single task. This was the fourth and final task in the study and was directed at the evaluation of the testbed facility developed in Task 3 and the accumulation of jitter data for a variety of input parameters. To be more definitive, Task 4 had the following subgoals:

- Gather jitter data for various parametric conditions. These data were tabulated and plotted for peak-to-peak and RMS jitter versus bandwidth, stuffing ratio, number of nodes, and tributary source offsets (up to ±200 bps).
- Confirm or deny analytical models by comparing the data collected in the above subgoal with comparable results of the analysis in Task 1.
- Reinforce the conclusions formulated during Task 1 as to the appropriateness of the recommended jitter specifications. This includes specifications on jitter accumulation on the output of single and multiple multiplexer/demultiplexer connections.
- Measure the susceptibility of the HN-74 to bit slips with respect to jitter as an input parameter to the bit timing recovery circuit.

SECTION 3.0

CATALOGING OF PULSE STUFFING MULTIPLEXER APPROACHES

3.0 CATALOGING OF PULSE STUFFING MULTIPLEXER APPROACHES

To insure that the pulse stuffing multiplexer jitter characteristics have been properly addressed it was first necessary to survey and catalog the various approaches to pulse stuffing multiplexers, to determine the mechanism of deployment for each approach, and to study the similarities and differences between approaches. This information formed the basis for building mathematical models to study pulse stuffing jitter. This three step effort, conducted as part of the intensive literature survey, served as the core of the Definition effort.

The survey revealed two basic types of pulse stuffing multiplexers:

(a) The positive-negative class whose data transport rate equals the mean channel data rate and which might lend themselves to supporting the eventual conversion to synchronous networks.

(b) The transport data rate offset class which was never intended to be part of a synchronous network but rather is used only in pulse stuffing multiplexer networks.

Since the first level multiplexer is the prime recipient of the jitter generated by the second level (pulse stuffing) multiplexers, it was necessary to direct a portion of the literature search to survey the bit synchronizer elements of a first level multiplexer. Review of these elements is necessary to establish criteria for tolerance on jitter and other characteristic parameters associated with pulse stuffing jitter.

3.1 Categories of Pulse Stuffing Multiplexers

The survey identified the following categories of pulse stuffing multiplexers and their definitions:

I. Transport Data Rate Offset Class

(a) Positive Pulse Stuffing (Positive Justification)

The provision for a fixed number of dedicated time slots (normally at regular intervals) in the transport digital signal marks this category. These time slots are being used to transmit either information from the tributary channels, or no information, according to the relative bit rates of an individual tributary channel and the transport digital signal. Additional inserted bits are deleted before the distributary channel is output.

(b) Negative Pulse Stuffing (Negative Justification)

The controlled deletion of bits from the tributary channel digital signal at dedicated time slot locations is characteristic of this category. The bit rates of an individual tributary channel correspond to the bit rate of the transport digital signal. The information content of the deleted bit is carried in an overhead bit of the transport digital signal and a bit containing this information is reinserted before the distributary channel is output.

II. Positive-Negative Class

(a) Positive-Zero-Negative Pulse Stuffing (Positive-Zero-Negative Justification)

This is a combination of the two prior techniques where the bit rate of the transport digital signal is usually equal to the mean tributary channel rate and either positive or negative stuffing is used depending upon the variation of the digital rate of the tributary channel. A no stuff (zero) command is used if no rate adjustment is needed.

(b) Positive-Negative Pulse Stuffing (Positive-Negative Justification)

This is an approach which differs from the prior one in that either a positive stuff or negative stuff command must be issued at every stuffing slot. Zero stuffing is achieved by alternating a positive and negative stuff. This approach only requires two commands - positive stuff and negative stuff.

3.2 Mechanism of a Pulse Stuffing Multiplexer

The second step in the literature survey was to postulate a pulse stuffing multiplexer mechanism model and to refine the model definition during the course of the literature search. This model is presented here to serve as a definition in the characterization of pulse stuffing multiplexer jitter.

The model involves three component elements - a multiplexer mechanism, a demultiplexer mechanism, and a smoothing loop mechanism. The multiplexer receives the tributary channel data into an elastic buffer. These data are input to the buffer under control of the tributary channel clock. The data are read out of the elastic buffer under control of the multiplexer's master clock. For each tributary channel a set of overhead digits and data buffer digits are carried on the multiplexers output stream. The overhead digits carry information to the demultiplexer such as frame sync, stuff bit status or control, and in the case of negative stuffing the information (polarity) of the deleted bit. The data transport digits are composed of data digits

and in the case of positive stuffing filler or stuff digits. The average rate that data are read out of the elastic buffer is the data transport digit rate. The instantaneous rate is the master clock rate divided by the number of tributary channels.

The decision to insert or delete (stuff) a digit is normally rendered by phase comparator circuitry which accompanies the elastic buffer in the multiplexer tributary channel input. This decision (stuff request) is rendered by the phase comparator when the phase difference between the buffer read and write clocks is off by one digit or greater. For the channel in question, the actual stuffing operation cannot occur until a stuffing opportunity occurs. Each tributary channel is allowed an opportunity to stuff periodically. Prior to this actual stuffing operation, the overhead digits must carry information to the demultiplexer as to whether a stuff will occur. In addition, for negative stuffing one of these overhead digits (the sense digit) actually represents the "stuffing opportunity." For this case, once a stuff request is acknowledged, the next sense digit is "loaded" by the next sequential data digit in the channel. Hence, it transports the information to the demultiplexer where it is removed and reinserted sequentially into the channels' data stream.

An exception to the prior discussed stuffing algorithm is that used by a positive-negative stuffing multiplexer. For a positive-negative multiplexer a deviation to this algorithm is required. In this multiplexer a positive and negative stuff are alternated every other opportunity when no stuff request exists. When a request for either a positive or negative stuff arrives, it is honored at the next possible stuffing opportunity. That is, when the next available proper stuff opportunity arrives, the alternating sequence is interrupted and the specific requested stuff is accomplished. The alternating sequence is then resumed.

In the demultiplexer the data transport digits are written into another elastic buffer at the data transport digit rate. The multiplexer-demultiplexer data transport communications are done synchronously so the master clock of the demultiplexer is synchronized to the multiplexer rate. When a positive stuff occurs, the stuff digit is deleted by inhibiting the write clock for that bit period. When a negative stuff occurs, accompanying circuitry obtains the data bit information from the sense digit and properly inserts it into the elastic buffer inbetween the other data digit writes.

The digits being written into this second elastic buffer are mesochronous with the original signal since all bits are being delivered and no bit accumulation build-up is occurring in the system. (Signals are mesochronous if their corresponding significant instants occur at the same average rate. Usually, the phase relationship between corresponding significant instants varies between specified limits.) The data being written into the buffer is at an instantaneous rate which is equal to the data transport digit rate. This rate is different from the original data rate of the tributary channel. The rates are made mesochronous by the dramatic discontinuities in the data stream (missing clock bits and double clock bits). This jittered clock rate is not acceptable for most devices (first level multiplexers, decryptors, etc.) Therefore, to remove the jitter or "smooth-out" the data, a phaselocked "smoothing" loop is used to read the data from the elastic buffer. Since data channels are plesiochronous among themselves, then each channel is required to have its own separate smoothing loop. The mission of the smoothing loop is not to track the signal, as is customary for phaselocked loops, but rather to attempt to duplicate a fairly stable source (the input signal). Consequently, the smoothing loop is picked to have an extremely "sluggish" response, and, hence, filter jitter induced by the discontinuities in the data stream.

The smoothing loop is driven by a signal derived from a phase detector which takes the difference from the elastic buffer write-clock (the jittered data transport digit rate) and the read-clock (the output of the loop itself). This error signal provides the stimulus necessary to drive and to hold the loop's digit rate at the average of the original input signal, thereby making both of those signals mesochronous. The literature survey identified a mixture of first order and second order loops used in this application. Some of the positive stuffing multiplexers used a first order loop. The positive-zero-negative multiplexer orignally used a first order loop for the prototype, but has since switched to a second order loop.

The following definitions and assumptions are derived from the model described above and are necessary to further define the study effort. These definitions have been selected to cover the broadest possible usage encountered in the literature search. Moreover, they are deemed necessary to this discussion to help arbitrate cases where either different terms or different interpretations appear in the literature. Part of the vocabulary differences arise in the literature where one specific pulse stuffing approach

was reviewed and no requirement existed to make these terms general to all four approaches.

Stuffing technique - the category of the pulse stuffing multiplexer (i.e., positive pulse stuffing, negative pulse stuffing, positive-zero-negative pulse stuffing, and positive-negative pulse stuffing).

Tributary channel input rate - the digit rate of an input channel, it is normally the output rate of a first level multiplexer.

Multiplexer output stream rate - the digit rate of the second level multiplexer output stream.

Output rate per tributary channel - the tributary channel contribution to the multiplexer output stream rate normally is equal to the digit output stream rate divided by the maximum number of tributary channels for the specific configuration. This is equal to the digit rate of the overhead digits and data transport digits associated with the operation of transporting that channel's information on the multiplexer output stream.

Overhead digits - the overhead digits normally consist of two district types:

housekeeping digits which are added, normally at regular time intervals to the digital signal to enable the equipment associated with the digital signal to function correctly, and possibly to provide ancillary facilities (i.e., frame marking, etc.)

stuffing service digits which transmit information concerning the status of the stuffing digit time slot and includes the sense digit (overhead digit which transports the information contained in the digit deleted from the tributary channel input stream in a negative stuffing situation).

Data transport digits - the data transport digits consist of the inclusive set of data digits and stuffing digits associated with transporting a given tributary channel input on the multiplexer output stream. Data digits consist of digits carrying the information of the tributary channel (Note, this excludes the sense bit.) Stuffing digits are redundant digits inserted in a stuffing digit time slot when that time slot does not contain a data digit.

Data transport rate - the average digit rate at which the data transport digits are moved on the multiplexer output stream. It should be noted that this rate is different from the instantaneous data transport digit rate. The instantaneous rate is equal to the multiplexer output rate divided by the number of tributary channels.

It was assumed that the study of the impact of overhead digits (their insertion in and deletion from the multiplexer output stream) on pulse stuffing multiplex jitter was beyond the scope of this effort. It is noted that the overhead digits are a fixed ratio of the data transport digits and that their rate is several times greater than the stuffing digit rate. Consequently, for the modelling done in this study, the data transport rate is assumed to be the instantaneous digit rate.

This assumption is one that has been made in most analyses discussed in the literature (Ref. 1,2,3). One study (Ref. 3) does discuss the effect of overhead digit operations on pulse stuffing multiplexer jitter.

Stuffable digit time slot - Either (a) a digit time slot for positive stuffing situations of the data transport digit which may contain either an information (data) digit or a stuffing digit or (b) for negative stuffing situations the respective location of a sense bit with respect to the data transport digits.

Stuffing opportunity - the arrival of a stuffable digit time slot in the digit stream.

Stuffing interval - the number of data transport digits per stuffing opportunity. (Note the interval includes one stuffable digit time slot).

Stuffing opportunity rate - the digit rate of arrival of stuffable digit time slots in the digit stream, which is normally computed by dividing data transport rate by the stuffing interval.

Stuffing rate - the rate at which stuffing digits are inserted or sense bits are actually employed. This is normally the absolute value of the difference between the data transport rate and tributary channel input rate. (Note that if the absolute value were not employed for a positive stuffing situation the true value of this rate would be positive while for a negative stuffing situation the value would be negative.)

Stuffing ratio - the ratio of the stuffing rate divided by the stuffing opportunity rate. (Note this is often explained as the number of stuffs to number of opportunities for a given time period.)

VCO Initial rate - This is the digit rate of frequency of the smoothing loop's undisturbed VCO. In a normal phase locked loop application, the frequency is offset to that of the input signal. In the smoothing loop application, the objective is to offset the frequency to the input rate of the tributary channel. The information of the tributary channel input is obtained from the jittered output of the demultiplexer which is mesochronous to it.

3.3 Survey of Pulse Stuffing Multiplexer Systems

A prime objective of the literature search was to establish present and proposed implementations of second level multiplexers. Findings of this search are outlined in Table 3.3. Proposed implementations described herein are recommendations found in the literature for future implementation. The table shows categories of pulse stuffing multiplexers and smoothing loops. Although they are elements of second level multiplexer systems, they truly

Table 3.3. Pulse Stuffing Multiplexer System State-of-the-Art

PULSE STUFFING MULTIPLEXER APPROACHES	SMOOTHING LOOP APPROACHES
POSITIVE STUFFING	ANALOG SMOOTHING LOOP
BELL SYSTEM M12	- FIRST ORDER LOOP
VICOM T1-4000	VICOM T1-4000
POSITIVE-ZERO-NEGATIVE STUFFING	BELL M12*
MARTIN-MARIETTA AN/GSC-24	- SECOND ORDER LOOP
POSITIVE-NEGATIVE STUFFING	AN/GSC-24 (PRODUCTION MODEL)
DISCUSSED IN THE CCITT PAPER (REF. 4)	BELL M12*
RECOMMENDATION G.741 BY THE U.S.S.R. AND AUSTRALIAN POST OFFICE	DIGITAL SMOOTHING LOOP
	- FIRST ORDER LOOP
	AN/GSC-24 (PROTOTYPE MODEL)
	- SECOND ORDER LOOP
	"UNIVERSAL SMOOTHING" LOOP PROPOSED FROM THE AN/USC-28 (MAGNAVOX RESEARCH LAB) BY COMPUTER SCIENCE CORPORATION.

*REF (2,5) indicates both first and second order analog candidates for the Bell M12.

are separate components and are often the subject of separate discussions. It is also noted that this constitutes two separate areas of investigation. The pulse stuffing approach addresses the area of synchronizing the basically asynchronous signals. The smoothing loop topic considers retiming the signal at the distribution end of the system.

3.3.1 Pulse Stuffing Multiplexer Approaches

There were three pulse stuffing multiplexers reviewed during the literature search - Bell M12, VICOM T1-4000 and Martin/Marietta AN/GSC-24. The first two use a positive pulse stuffing approach. The third one uses a positive-zero-negative pulse stuffing approach. In addition, the recommendation in the CCITT by the U.S.S.R. and the Australian Post Office for a positive-negative approach was reviewed. The decision, as a result of this literature review, was that this study should address the positive stuffing approach and the positive-zero-negative approach. While the literature was very enthusiastic about the positive-negative approach, it was considered that an analysis of this approach was beyond the scope of the present study.

Table 3.3.1 shows a brief comparison of the three implemented approaches. The Bell M12 is a 4-channel multiplexer. For the VICOM T1-4000 a 4-channel version of the second level multiplexer was selected. The AN/GSC-24 is a versatile machine which can accept inputs ranging up to 3 MHz. The characteristics shown in the table are those selected for one configuration which closely matches the other two multiplexer configurations. While the summary shows differences between the three multiplexers, it is necessary to discuss the multiplexed output stream data formats of each so that better insight can be attained as to the actual operation of a pulse stuffing multiplexer.

3.3.1.1 Bell M12 Multiplexer Output Stream Frame Format

Figure 3.3.1.1 shows the format of the M12 multiplexer (Ref. 5). The tributary input channels are defined to be Bell T1 channels. In the format after every 48 information time slots, 12 from each of the four T1 signals, a control digit is inserted by the multiplexer. During the frame, each signal has 288 (12x6x4) positions, and the overhead structure permits one stuff bit. Control digits labeled F are the main framing digits. Between F digits are control digits labeled M and C. Three successive C digits denote the presence or absence of

Table 3.3.1. Comparison of Existing Second Level Multiplexers

	BELL M12	VICOM T1-4000	MARTIN AN/GSC-24
Stuffing Technique	POS.	POS.	POS.-ZERO-NEG.
Number of Tributary Input Channels	4	4	27 Ports (6 Ports/Ch.)
Tributary Channel Input Rate (Nominal) (MHz)	1.544	1.544	1.536
Input Channel Offset Tolerance (Hz)	+150, -300	+150,-300	+384,-384
Multiplexer Output Stream Rate (MHz)	6.312	6.2763	7.168
Data Transport Rate (MHz)	1.545796	1.544935	1.536000
Major Frame Size	1176	2340	25172
Minor (Sub) Frame Size	294	130	812
Overhead Digit/Data Digit Structure	6/288	2/128	29/783
Stuffing Interval	288	576	889
Stuffing Opportunity Rate (Hz)	5367	2680	1727
Stuffing Ratio (Nominal)	0.3346	0.3486	0.00
Stuffing Ratio (+ Offset)	0.3067	0.2927	0.22225
Stuffing Ratio (- Offset)	0.3905	0.4604	0.22225
Smoothing Buffer Size (Bits)	4	3	

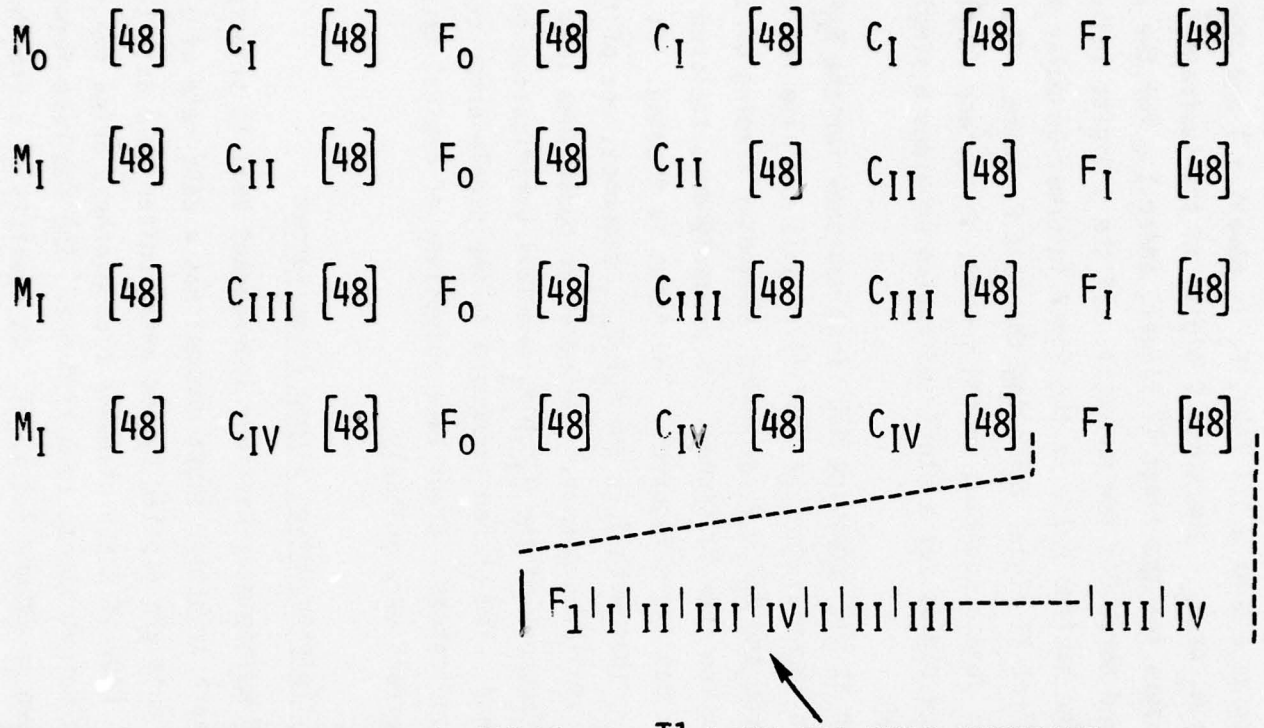


Figure 3.3.1.1. Bell M12 Multiplexer Frame Format

of a single stuffed pulse, and the corresponding M digit identifies in which of the four multiplexed T1 signals the stuff occurs. The M digits thus form secondary framing digits and identify four subframes. The subscripts of the M and F digits identify the digit as a 0 or a 1. Thus, F_1 is always a 1 and the next control digit is either an M_1 or M_0. The three C digits in the subframe following M_0 are stuffing indicators for the first T1 signal, three 1's for the presence of a stuffed pulse and three 0's for no-stuff. If the C digits indicate a stuff, the location of the stuffed pulse is the first information pulse position associated with the first T1 signal following the next F_1 pulse. The other sequences of C digits denote stuffing in the second, third, and fourth T1 signal. The use of three digits for a stuff indication provides a single digit error correction code.

The demultiplexer at the receiving M12 first searches for the $F_0F_1F_0F_1$ sequence. This establishes identity for the four T1 signals and also for the M and C control digits. From the $M_0M_1M_1M_1$ sequence, secondary framing of the C digits is established and the four T1 signals are properly demultiplexed and destuffed. This format has two safeguards. The first is framing. It is possible, although unlikely, that with just the $F_0F_1F_0F_1$ sequence, one of the T1 signals could contain a similar sequence. The receiver could then lock onto the wrong sequence. Presence of the $M_0M_1M_1M_1$ provides verification of the genuine $F_0F_1F_0F_1$ sequence. The second safeguard is the single error correction ability of the stuff indicators. Error rate objectives of digital transmission lines make double errors very unlikely.

3.3.1.2 VICOM T1-4000 Multiplexer Output Stream Frame Format

The VICOM T1-4000 multiplexer has four independent Bell T1 tributary input channels (Ref. 6). Each tributary input channel has a data rate of 1.544 MHz (+150,-300 Hz). These data are stuffed by the synchronizer to a data transport rate of 1.544935 MHz. Four of these channels plus overhead bring the total digit rate of the multiplex output stream to 6.2763 MHz. The subframe format for this multiplexer is shown in Figure 3.3.1.2-1. It consists of a framing bit (BF), 16-four bit words (one bit from each channel), a control bit (BC) and 16-four bit words for a total of 130 bits. The framing bit is an alternating ONE-ZERO pattern. The control bits provide a control channel for transmission of stuffing information; that is, the control bits from 18 sequential subframes form

the 18-bit control frame channel shown in Figure 3.3.1.2-2. For each T1 channel there are 2,680 timeslots per second located at specific times in the frame which may contain either T1 data or a stuffed pulse. The occurrence of stuffed pulses in these locations is flagged by data in the control channel. A six-bit marker word is used at the start of each frame for framing.

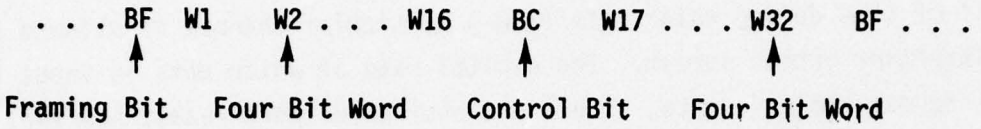


Figure 3.3.1.2-1. Subframe Format for the Four-Port Multiplexer

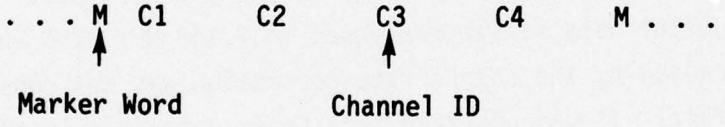


Figure 3.3.1.2-2. Control Channel Frame
for the Four-Port Multiplexer

The C words are 3-bit channel ID's for indicating the presence of stuff bits in a given channel. They are redundantly coded (000 - not stuffed, 111 - stuffed) so that link errors can be corrected. Each of the C words supplies information on the possible stuff timeslots which will occur in one particular word of the 32 words transmitted between the second and third marker bits. This information is used at the demultiplexer to perform the destuffing operation.

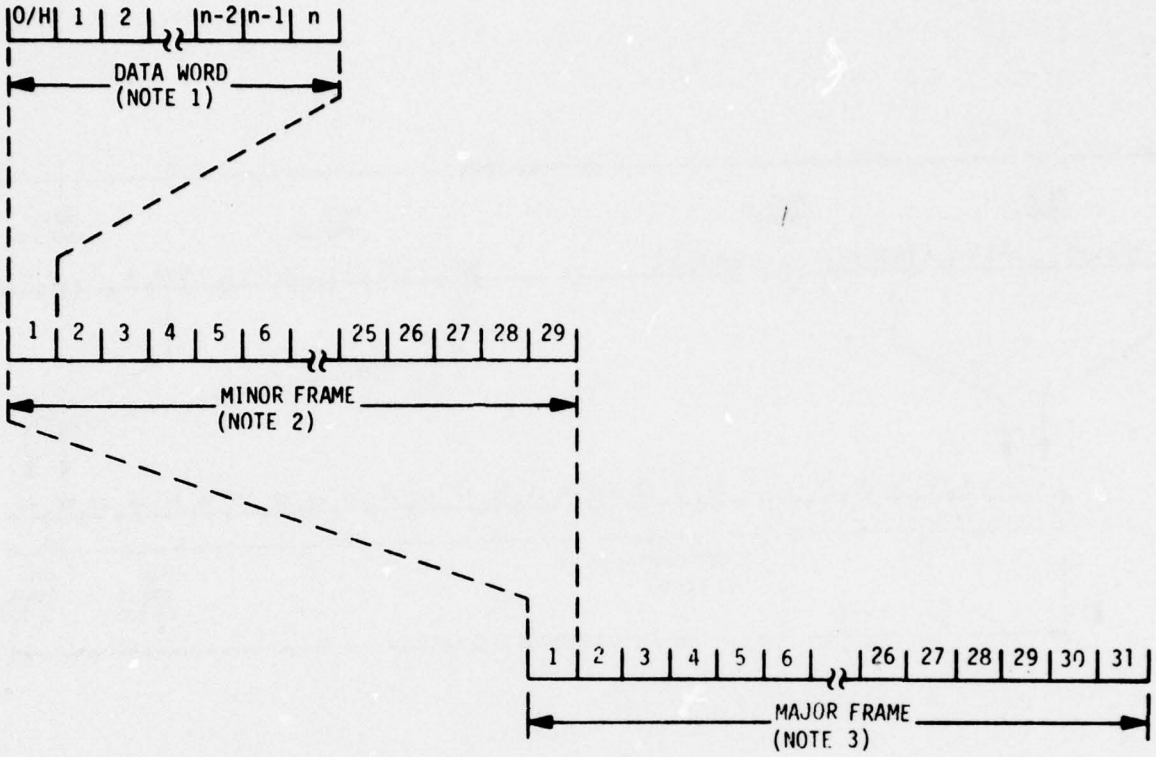
3.3.1.3 Martin/Marietta AN/GSC-24 Multiplexer Output Stream Frame Format

The AN/GSC-24 is an extremely versatile machine (Ref. 7). It can function both as a first level multiplexer and a second level multiplexer. It is structured around a concept which uses ports for combining tributary channel inputs into a single multiplexer output data stream. Several ports can be strapped together to transport the tributary channel's data. Coarse rate correction can be applied to the port-strapped configuration to allow handling of data which is at other than a multiple of the basic port rate. Simply stated, a port is an interval of time during which data from a particular channel is allowed into the multiplexer output stream. The digital rate at which data is input to a port is termed the port rate. There are choices of port rates; however, when established for a given multiplexer, the port rate remains constant for all ports in use.

For the AN/GSC-24 described in Table 3.3.1, a tributary input channel rate of 1.536 MHz (±384 Hz) was selected. The port rate selected for that multiplexer was 256 kHz. Consequently, six ports were required to handle the tributary input channel. The channel rate was a multiple of the port rate so no coarse correction was needed for that channel. In addition, the multiplexer described had a total of 27 ports in use plus the overhead port. Consequently, the multiplexer output data stream was equal to 7.168 MHz (256 kHzx28). The study of jitter caused by the coarse rate correction was not considered part of this study effort. It was observed that tests described in the literature (Ref. 8) were concerned with jitter created via coarse correction.

The multiplex output stream message format for the AN/GSC-24 is shown in Figure 3.3.1.3-1. Each multiplexer configuration must use a minimum of 15 ports, therefore, the minimum data word length is 16 bits and can range up to 32 bits when all 31 ports are in use. A minor frame contains 29 data words and one complete 29-bit overhead message. Figure 3.3.1.3-2 shows the organization of the overhead message. Each minor frame provides the necessary control which permits the stuffing of the port addressed by that minor frame. Although it was not clear from the documentation reviewed, it is implied that each minor frame within a major frame permits a unique port to be stuff. That is, it is implied that a given port can be stuffed only once a major frame.

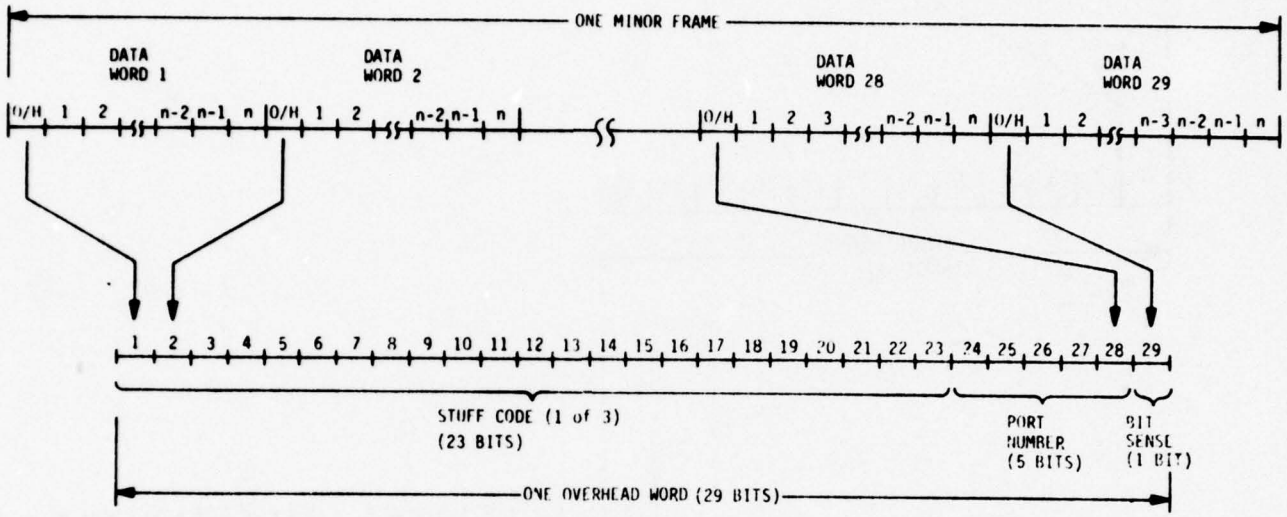
The overhead message, shown in Figure 3.3.1.3-2, consists of a 29-bit word, with one bit located in the first bit position of each of the 29 data words, comprising the minor frame. The overhead conveys three types of information: a



NOTES:

1. EACH DATA WORD CONTAINS ONE OVERHEAD (O/H) BIT PLUS ONE DATA BIT FOR EACH USED PORT. TOTAL NUMBER OF WORD BITS FOR A GIVEN CONFIGURATION IS BETWEEN 16 AND 32.
2. EACH MINOR FRAME CONTAINS 29 DATA WORDS. AN O/H BIT FROM EACH DATA WORD MAKES UP ONE 29-BIT O/H WORD PER MINOR FRAME.
3. EACH MAJOR FRAME CONTAINS 31 MINOR FRAMES.

Figure 3.3.1.3-1. AN/GSC-24 Multiplexer Frame Format



NOTE: VALUE OF n IN DATA WORD IS BETWEEN 15 AND 31

Figure 3.3.1.3-2. Overhead Message Format

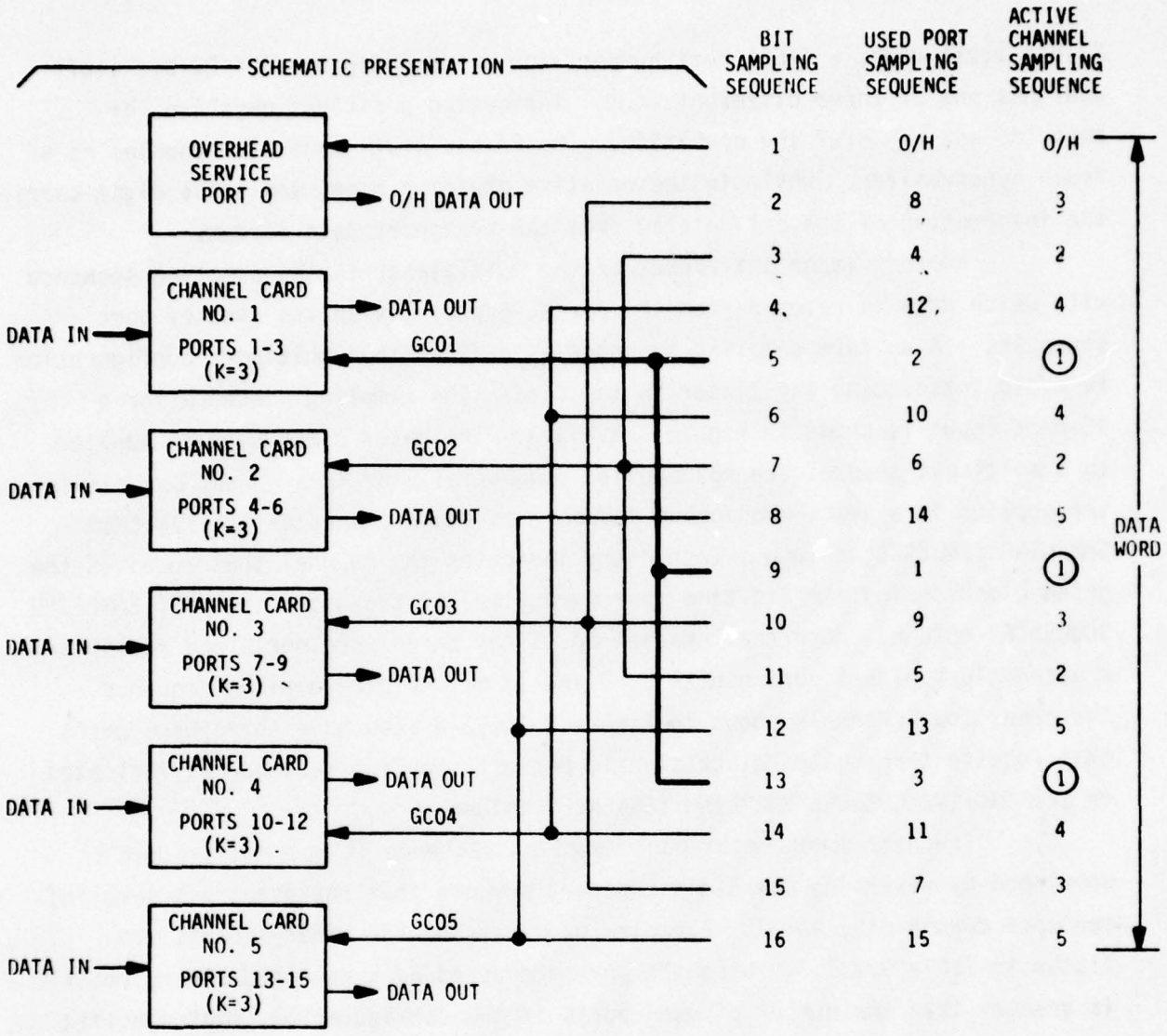
23-bit stuff code, a 5-bit port number, and a sense digit. The 23-bit stuff code has one of three different forms, indicating positive, negative, or zero (no-action) stuffing operation. The 23-bit stuff code also doubles as a frame synchronizer. While in the negative stuffing mode, the sense digit carries the information of the bit deleted from the transport data stream.

Another important aspect of the multiplexer is the sampling sequence with which data is removed from the ports, especially in the case of port strapping. A uniform sampling sequence is desired in a multiport configuration to avoid introducing any jitter to the data. The sampling sequence for a 15-port input is shown in Figure 3.3.1.3-3. The gated clock signals applied to a multiport channel are not applied sequentially or in a group, but rather are applied in a near homogeneous sequence as shown under the "ACTIVE CHANNEL SAMPLING SEQUENCE" column. Each entry indicates the channel that receives the gated clock during the bit time (per word time) listed under the "BIT SAMPLING SEQUENCE" column. Note that channel No. 1 has three used ports and receives a gated clock signal during bits 5, 9 and 13 of the bit sampling sequence. The other four channels shown in Figure 3.3.1.3-3 also have three used ports that receive three gated clock signals per bit sampling sequence as indicated in the "ACTIVE CHANNEL SAMPLING SEQUENCE" column.

The near homogeneous port sampling sequence is not random, but is developed by reversing the 5-digit binary numbers that represent bit sampling sequence counts of 1 to 31. Examples of reversing the binary counts are listed in Table 3.3.1.3. When the port addressed by a reversed binary count is greater than the number of used ports in the configuration, that specific address is automatically bypassed and the next applicable port count is generated without any delay. The following example assumed that the system used 15 ports. The use of reverse binary weighting to achieve near homogeneous gating simplified the logic implementation required for extracting data from the channel cards.

For the purpose of modelling the AN/GSC-24, the sampling sequence was assumed to be homogeneous. The jitter frequency attributed to the near homogeneous sampling is considered to be systematic and of relative high frequency somewhat equivalent to that of overhead bit deletion.

The problem of homogeneity of the stuffing interval in a multiport application was of interest to this effort. However, the literature reviewed



NOTES:

1. TYPICAL CONFIGURATION: DATA WORD CONTAINS 16 DATA BITS (ONE O/H BIT PLUS ONE BIT PER PORT).
2. K-3 INDICATES THREE USED PORTS REQUIRED TO SERVICE ONE CHANNEL.
3. ○ SHOWS HOMOGENEOUS SAMPLING SEQUENCE FOR CHANNEL CARD NO. 1 WITH USED PORTS 1, 2, AND 3.

Figure 3.3.1.3-3. Example of Homogeneous Sampling Sequence

Table 3.3.1.3. Port Sampling Sequence

Decimal Count	Binary Count	Reversed Binary Count	Resultant Decimal Count	Used Port Sequence	Associated Channel Sequence
1	00001	10000	16	Bypass	
2	00010	01000	8	8	3
3	00011	11000	24	Bypass	
4	00100	00100	4	4	2
5	00101	10100	20	Bypass	
6	00110	01100	12	12	4

did not reveal such information. It was therefore concluded that a reverse binary sequence was possibly used to establish what port would be addressed during a given minor frame and that a near homogeneous sequence would be developed. A homogeneous sequence was assumed for the model of the AN/GSC-24 to make it compliant to the other multiplexer models. However, this area should be considered for possible jitter contributions in future investigations.

3.3.2 Smoothing Loop Approaches

There were four implemented smoothing loops discussed in the literature and one proposed implementation. The literature survey revealed that first order analog smoothing loops are used with the VICOM T1-4000 and the Bell M12; a second order analog smoothing loop was used in the AN/GSC-24 production model. A first order digital smoothing loop was implemented as part of the prototype AN/GSC-24. A second order digital loop used by Magnavox Research Laboratories in the AN/USC-28 was considered in a study by Computer Sciences Corporation to improve the smoothing performance of the AN/GSC-24. This proposed implementation is labelled the "Universal Smoothing Loop" because according to the CSC literature it achieves uniform smoothing over the entire range (50 Hz to 3 MHz) (Ref. 9).

Third order loops, because of two integrators, eliminate steady state acceleration errors. This property would be desirable in tracking an accelerating signal - such as a Doppler signal from a satellite - since should the signal momentarily fade out the loop would continue tracking the phase

accelerating (frequency velocity) signal. However, application of accelerating signals such as Doppler were not considered within the scope of this study and consequently the smoothing loop was restricted to first and second order.

Of particular interest to this study was the specific value of the smoothing loop parameters, specifically, the loop gain in the case of a first order and the lead and lag parameters in the case of a second order loop. In addition, for the phase detector the value of K_d (phase-detector gain factor) and the number of bits used in the elastic buffer would be desirable to model the specific smoothing loop. Also, for the VCO the value of K_o (VCO gain constant), its operating range, and the value of the VCO natural frequency are important. However, most of this information was not available in the literature reviewed. The VICOM T1-4000 circuit schematic was available, but specific component values were not available (Ref. 6). A task to obtain such information was considered beyond the effort expected during this study. Ref. 2 limited various Bell M12 loop parameter values. Information on other loops was not available to this level of detail. The simulation models were designed with the smoothing loop gain parameters as variables of simulation and expected value ranges were used for analysis purpose.

Theoretically, the prime difference in the transfer function of the smoothing loop is between a first and second order loop. Considerations of sampled-data theory indicate that for such an oversampled system the digital and analog approaches would yield similar results. However, one practical implementation of a digital VCO does yield a design which varies the frequency by digitally slicing pulses and, consequently, contributes jitter by this phase step change.

The software simulation was designed using a classic analog approach to simulate both a first and second order loop. This analog approach was selected to take advantage of the adaptive step-size integration of the simulation tool to gain program execution speed. The digital loop simulation could be an extension to the software simulator. A digital approach was selected for the hardware simulator. This choice was based on the requirement to vary the loop parameters over a range of values. A digital first order loop was selected for the hardware simulation with the capability of expansion to a second order loop by inserting lead-lag filter cards.

3.4 Survey of First Level Multiplexer Systems

The AN/GSC-24 Second Level Multiplexer can also be configured to function as a first level multiplexer. As such it would receive and operate with the jittered distributary channel output from the second level multiplexer. In keeping with the scope of this program, the study was limited to the TSEC/CY-104 First Level Multiplexer, in particular, the HN-74 Interface Equipment which is the I/O unit to the Second Level Multiplexer. It is considered that this system would serve as an adequate model to create tolerances for the jitter generated by the pulse stuffing multiplexer.

This first level multiplexer accepts audio and signalling information (8 kHz) from 24 input channels and performs the processes of digitizing, multiplexing and encryption to provide a Bell T1 tributary channel output data stream. It also accepts a T1 input data stream and performs the function of bit time recovery, decryption, demultiplexing and analog conversion to produce the output audio channels.

The TSEC/CY-104 consists of three basic components: the HY-12 wideband PCM Trunk Carrier Equipment, the KG-34 Secure Key Generator, and the HN-74 Signal Interface and Control Unit. A block diagram of the CY-104 is shown in Figure 3.4-1.

The HY-12 time division multiplexes 24 voice channels. Using an 8-bit PCM with companding, it samples each channel at an 8 kHz rate, adds overhead, and produces a 1.544 MHz serial bit stream. Timing jitter effects the HY-12 demultiplexer while reconstructing voice waveforms in each channel. However, preliminary investigations show the effect to be negligible compared to the bit synchronizer problem. The study was not directed to investigations in this area.

The KG-34 encrypts/decrypts the data. This crypto interface is a sensitivity point in the first level multiplexer where clock jitter and clock duty cycle variations can affect the ability of the cryptographic device to perform in a reliable manner. In a more comprehensive study, the detailed timing requirements of the KG-34 should be considered to guarantee that accumulated jitter does not cause the KG-34 to lose synchronization. However, in this preliminary study it was necessary to simplify the objectives by concentrating only on the bit synchronizer.

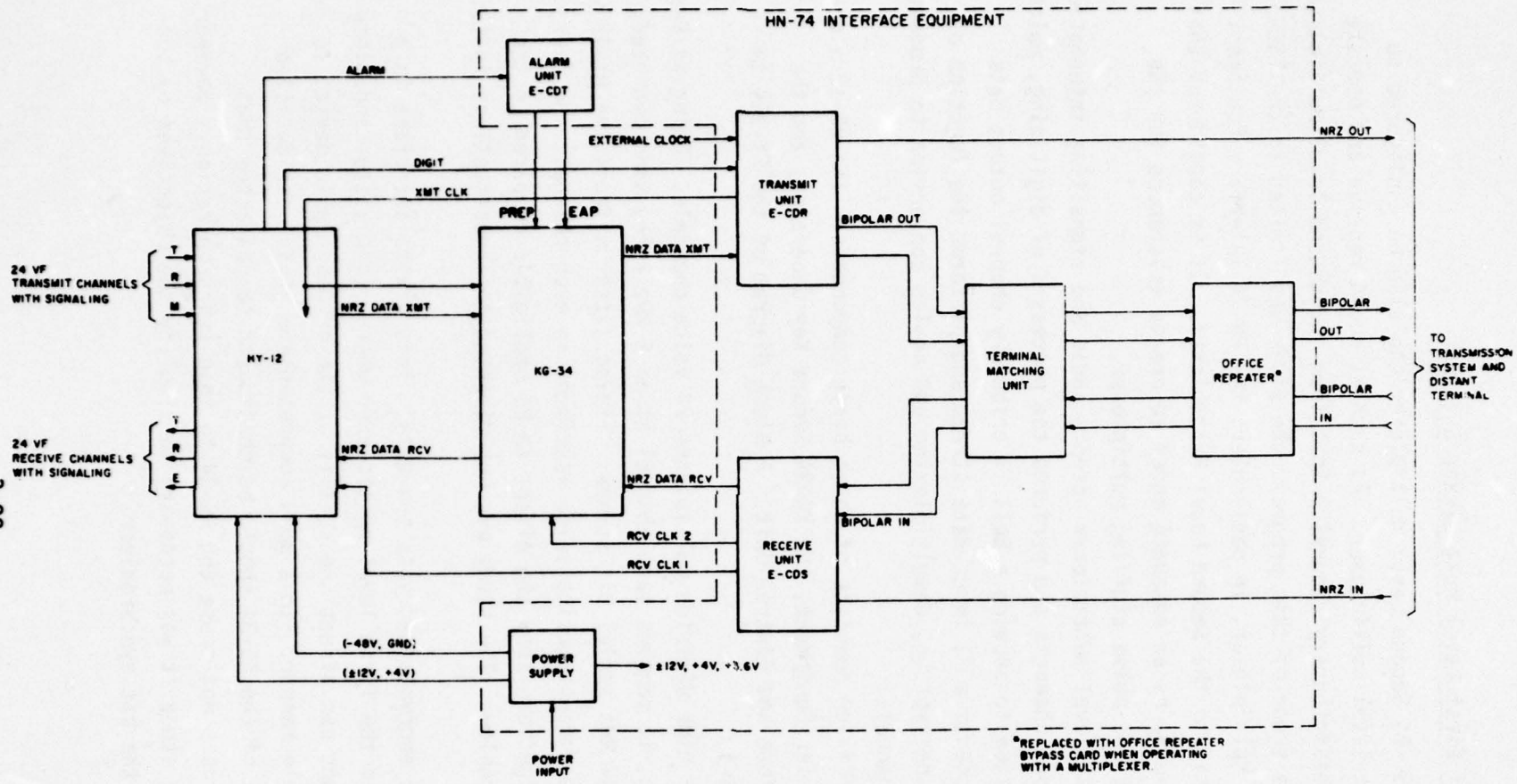


Figure 3.4-1. TSEC/CY-104 System, Block Diagram

The HN-74 Signal Interface and Control Unit prepares the data for transmission in a compatible NRZ or Bipolar format (Ref. 10). This unit is important to the operation of the first level demultiplexer since the HN-74 E-CDS Receive Unit accepts the input distributary channel and derives bit timing from it. The first level multiplexer's sensitivity to input jitter in the bit timing recovery circuits is in terms of bit count integrity or bit slips. If bit slips occur the result is loss of crypto sync, demultiplexer sync, and, hence, all audio communications.

The E-CDS Receive Unit of the HN-74 reconstructs bit timing with a phase-locked loop. The basic functions of this loop are indicated in Figure 3.4-2. The one shot and gate act as the phase detector for this loop and the integration is accomplished by charging or discharging a capacitor. The clock is a crystal oscillator controlled by a variable capacitance diode.

The operation of the bit timing recovery circuit is described as follows. When the loop is locked, the one shot, which is triggered by data transitions, allows the gate to be opened a small time centered about the clock transition. This gives no net change to the capacitor charge. A small phase change between the data and clock increases (or decreases) the capacitor charge and appropriately changes the clock rate. For a positive going transition the data, one shot, clock and phase characteristic are shown in Figure 3.4-3.

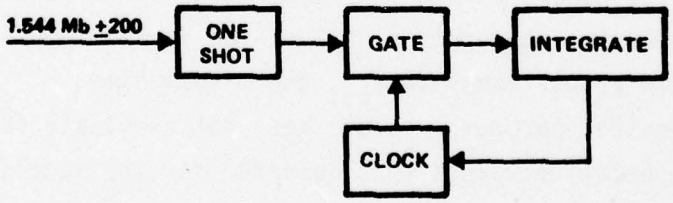


Figure 3.4-2. HN-74 Timing Recovery Loop

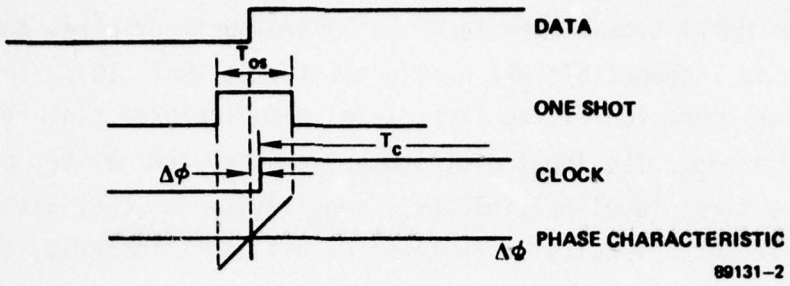


Figure 3.4-3. HN-74 Bit Time Recovery Operation

Note that the desired linear phase characteristic exists only over the one shot time duration, T_{os}. This is the limiting factor on the amount of total phase jitter this system can allow.

The remaining portion of the configuration corresponds to a second order phased-lock loop which is standard in bit synchronizers. An important characterization of this is its closed loop bandwidth which is a function of the capacitor charging time constant, the one shot time duration, and the loop gain constants. The phase locked loop circuitry maintains the clock frequency in precise synchronization with the incoming digital data stream rate. The ability to track the incoming digital signal is a function of the loop bandwidth. Therefore, the loop bandwidth is a major factor in the timing jitter tolerance considerations for this study.

The model generated for the synchronizer is a second order loop with a window postulated for the error signal of the locked loop. The width of this window is directly proportional to T_{os}, the window time.

The specific parameter values were not available from the literature. A range of representative values were selected for the models exercised.

SECTION 4.0

PULSE STUFFING MULTIPLEXER ANALYSIS APPROACH

4.0 PULSE STUFFING MULTIPLEXER ANALYSIS APPROACH

The objectives of this analysis effort were to characterize pulse stuffing and waiting time jitter and to determine the additional effect, if any, on jitter created by tandeming pulse stuffing multiplexers. Furthermore, additional motives were to apply this information to analyze and evaluate models of existing hardware and to broaden overall understanding of the pulse stuffing environment so that realistic jitter specification techniques could be derived. The approach taken to accomplish such an analysis was to develop three tools: an analytical model, a software simulator, and a hardware simulator. The analytical tool provided the basis to guide the effort; the software simulator provided the depth to analyze the continuous-time system with varying discrete-time inputs; and the hardware simulator rendered to the study the hardware confirmation of the results and added the depth that is often omitted from pure analysis. In addition, the interplay between the three tools provided growth to each tool, and the combination contributed to a more indepth understanding of the problem.

4.1 Analysis Approach

An understanding of the characteristics of pulse stuffing multiplexer operation indicate that there are two elements which contribute to the multiplexer jitter. The jitter created by these two elements is defined as follows:

- Stuffing jitter which results from the insertion or deletion of bits to or from the data transport digit stream.
- Waiting-time jitter which results from the situation that a pulse is not inserted/deleted when the phase difference between the data transport digit stream and the tributary input stream has changed by a bit but rather the stuffing operation is delayed until the next stuffable digit time slot.

In addition, any element of jitter contributed by the tandeming of pulse stuffing multiplexers is defined as cascading jitter. It is desirable to understand the elements that influence each of these jitter types so that specific control on each type can be exerted by the generated jitter specification technique.

The literature search disclosed that previous analysis efforts (Ref. 1,2,3) have been performed using the classic spectrum analysis approach. In this approach the spectrum of the jittered waveform is derived by formulating the spectrum of the

unfiltered jitter and, then, multiplying it by the response of the smoothing loop. In addition, calculations based on the theoretical jitter spectrum are used to show, under given conditions, the upper bound on the rate at which the RMS amplitude of the cascaded jitter grows. These theoretical calculations were backed-up by test results derived from experiments with actual hardware.

Difficulty in using these results directly was encountered in relating the results to the various control parameters. The model was complex to begin with, varying given parameters was intricate and, furthermore, the results were difficult to interpret with respect to the parameter of interest. In addition, the analysis did not attempt to establish differences between stuffing jitter and waiting time jitter. Instead, it elected to deal with the combined jitter spectrum. The conclusion was reached at program onset that complementing the existing analysis with a time domain analysis might be a more fruitful approach to pursue. This conclusion has been strengthened by the following four facts:

a) It is easier with the time domain analysis and the simpler model to gain insight into the jitter phenomena. Such insight is indispensible in a trade-off study.

b) The time domain analysis provides information on RMS jitter, peak-to-peak jitter, and jitter slew rates; the spectrum analysis only provides information on RMS jitter.

c) Results predicted by both models are substantially in agreement.

d) When model complexity is required, it can be easily accommodated by the time-domain software simulator.

4.1.1 Phase Jitter Models

The analysis effort started from two fundamental phase jitter models - the first describing the stuffing jitter components, and the second describing the waiting-time jitter component. The stuffing jitter model is delineated first.

The jittered waveform prior to the smoothing loop is inputted to the elastic buffer by the demultiplexer (which either removes or inserts digits as required to invert the synchronizer operation of the pulse stuffing multiplexer). The waveform for a positive stuffing system is depicted in Figure 4.1.1-1. The upper graph shows the cumulative phase relationship as a function of time for the tributary input channel and the unfiltered distributary output channel. The slope of the unfiltered output channel cumulative phase waveform is equal to the

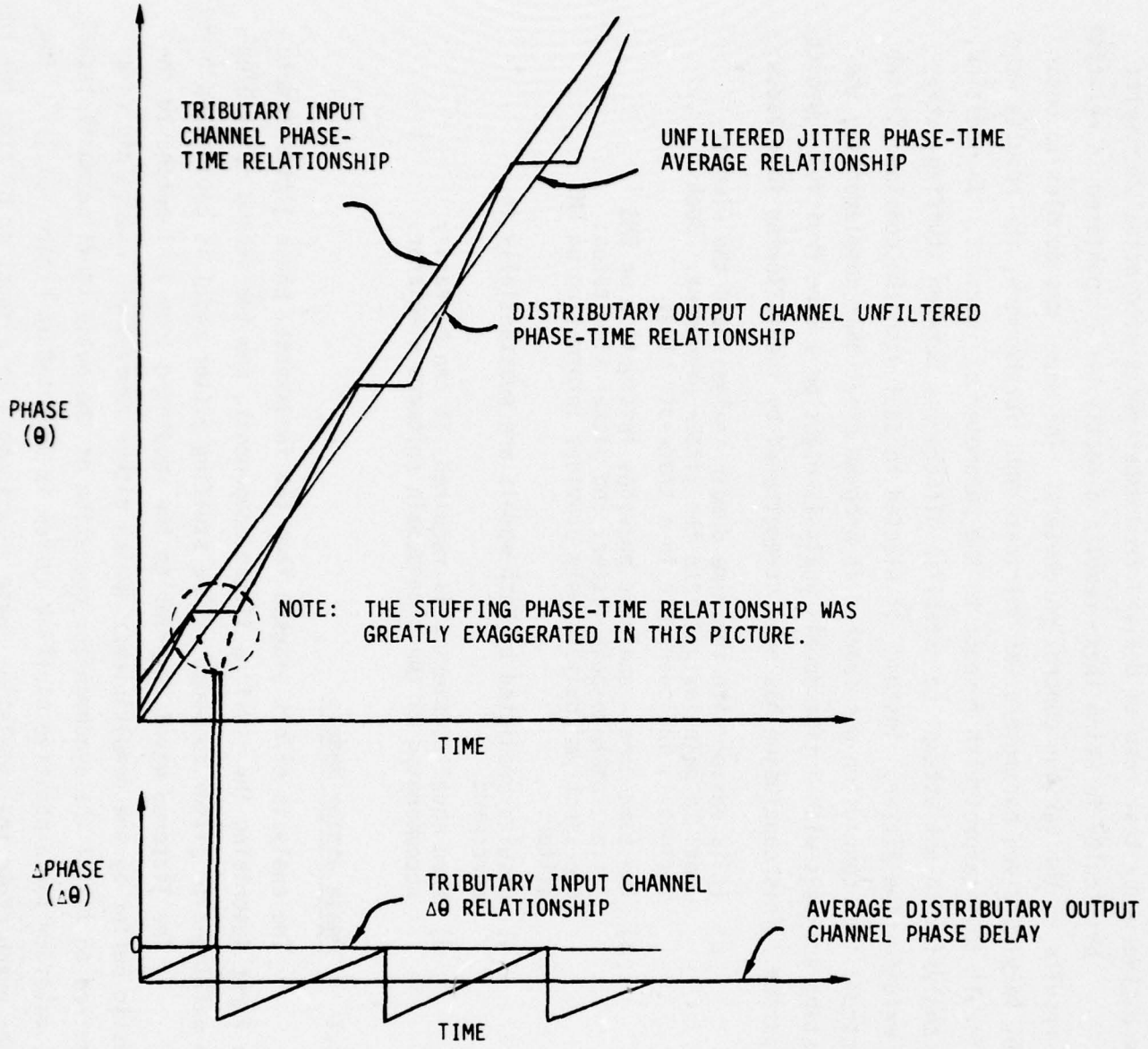


Figure 4.1.1-1. Model for Unfiltered Stuffing Jitter
(Positive Stuffing System)

digital rate at which data is being written into the elastic buffer. It is normally equal to the data transport rate except when the write clock is halted by the operation which deletes a stuffed bit. Since the stuffed digits are added to synchronize the input channel, on removal of these digits the average rate is equal to the average rate of the input channel (the two are mesochronous). In the elementary model shown in Figure 4.1.1-1, the tributary input channel is assumed to have a constant input digital rate. The quantization effect of digital transfer is ignored except for the stuffed bit, constant time delays between the input channel and output are not shown, and waiting-time effect is not considered.

The jitter effect is the difference between the output channel and the input channel, which is assumed for this case to be a stable (isochronous) digital rate. From this observation, the conclusion is drawn that the difference ($\Delta\theta$) model provides the phase jitter information. In this delta phase ($\Delta\theta$) model, the slope of the sawtooth is equal to the difference in rate between the data transport rate and the tributary input channel rate. The period of the sawtooth is equal to the stuffing rate. The peak-to-peak value is one bit (the stuffed bit). Because a sawtooth waveform has a uniform amplitude distribution, the RMS value attributed to this jitter should be $1/\sqrt{12}$ bits.

The next model is the waiting-time jitter model. For the jitter waveform to be the periodic sawtooth model described in the above paragraph, the stuffed bit would need to be inserted at the specific instant that the phase error crossed a threshold. That is, the stuff interval would have to be an integer number of stuffing opportunities. However, if this is not the case, an additional phase jitter is generated. This additional jitter called waiting time jitter, denoted by the dashed lines of Figure 4.1.1-2, may also be modeled as a sawtooth waveform which has a functional frequency equal to the beat between the stuffing rate and a subharmonic of the stuffing opportunity rate (maximum stuffing rate). Figure 4.1.1-3 depicts how the peak value of waiting time jitter may be computed. If the phase error crosses the threshold immediately after an available stuffing slot, then the error will accumulate until the next possible stuffing time. The amount of phase which can accumulate during this interval equals the frequency offset times the interval between available stuffing slots.

$$\varepsilon = f_o \, t_s \text{ bit slots} .$$

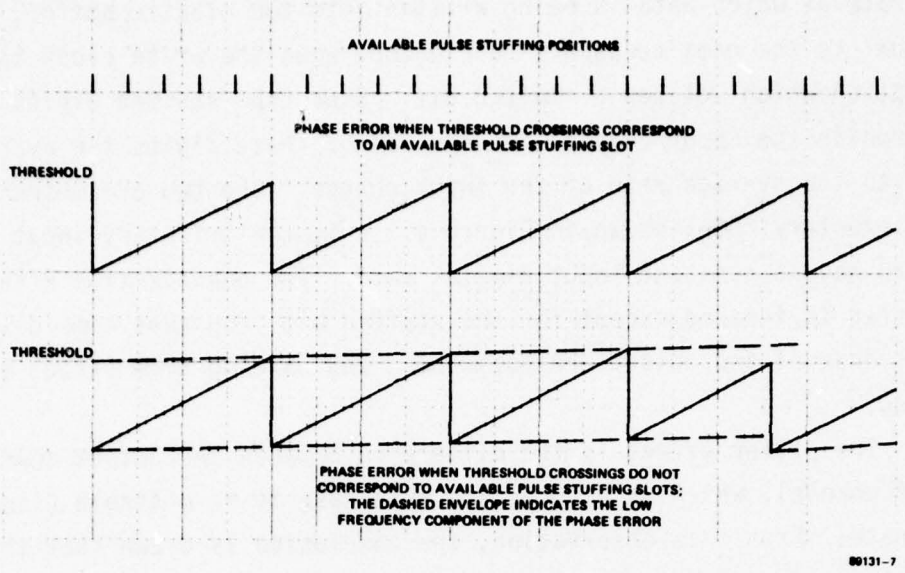


Figure 4.1.1-2. Waiting Time Jitter

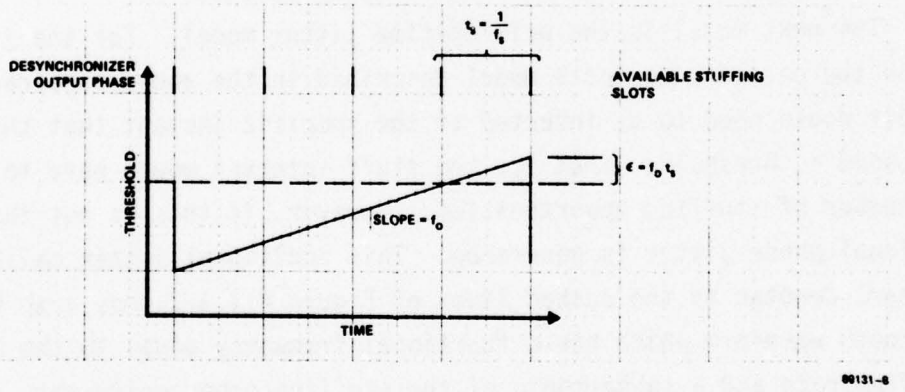


Figure 4.1.1-3. Peak Value of Waiting Time Jitter

The offset frequency f_o, which is the slope of the sawtooth, is some fraction of the stuffing opportunity rate f_s $\left(f_o = \frac{f_s}{n}\right)$. The stuffing ratio is defined as the ratio of the stuffing rate divided by the stuffing opportunity rate, $\rho = \frac{f_o}{f_s}$. Thus, the maximum phase accumulation above the threshold is

$$\varepsilon = f_o t_s = \rho f_s t_s = \rho \text{ bits} .$$

Since a stuffing slot might be available at the time the phase crosses the threshold, the minimum excess phase is 0. Therefore, the unfiltered peak-to-peak waiting time jitter is

$$\varepsilon = \rho \text{ bits} .$$

The maximum RMS value of this jitter should, therefore, by reason of the sawtooth waveform model equal $\rho/\sqrt{12}$, if phase offset is removed.

4.1.2 Smoothed Output Jitter Models for First Order Loop

The analysis effort was next directed to study the effects of a first order smoothing loop on the jittered waveform. The analysis was aimed at the stuffing jitter waveform since it was observed to be periodic. In the case of positive (or negative) stuffing, the stuffing rate is normally large enough to be attenuated by the smoothing loop. It was intuitively felt that this area was influenced most by the smoothing loop.

The output jitter waveform may be computed by convolving the smoothing loop phase impulse response with the sawtooth phase jitter waveform ($\Delta\theta$) which represents the unsmoothed jitter. The closed loop frequency transfer function of a first order smoothing loop (Ref. 11) is

$$H(\omega) = \frac{\omega_c}{\omega_c + j\omega} .$$

The corresponding impulse response is

$$h(t) = 2\pi f_c e^{-2\pi f_c t} ,$$

where f_c is the 3 dB cutoff frequency of the smoothing filter. Herein f_c is expressed in percent of the stuffing rate. The periodic sawtooth waveform with a period of -0.5<t<0.5 is written as

$$\omega(t) = t-n. \qquad -0.5-n<t<0.5-n$$

$$n=0, \pm1, \pm2, \ldots$$

The result of the convolution of the first-order smoothing loop with the periodic sawtooth waveform is

$$y(t) = \int_{-\infty}^{t} \omega(\alpha)\ 2\pi f_c e^{-2\pi f_c(t-\alpha)}\, d\alpha \ .$$

Upon carrying out the integration, the output jitter over the output period -0.5<t<0.5 is

$$y(t)=t-\frac{1}{2\pi f_c} + e^{-2\pi f_c t}\ \frac{e^{-\pi f_c}}{1-e^{-2\pi f_c}} \ .$$

This waveform has a maximum value at the two extremes (t=±0.5) and a minimum point in between. The minimum point is located at

$$t = -\tfrac{1}{2} + \frac{1}{2\pi f_c}\ \ln\left(\frac{2\pi f_c}{1-e^{-2\pi f_c}}\right).$$

Using this value, the peak-to-peak output jitter is expressed as

$$\Delta y_{p-p} = \frac{1}{(1-e^{-2\pi f_c})} - \frac{1}{2\pi f_c}\ \left[1+\ln\left(\frac{2\pi f_c}{1-e^{-2\pi f_c}}\right)\right].$$

Continuing with the exercise, the RMS equation is derived next. First, the jitter average is computed over a period (T=1).

$$\overline{y(t)} = \frac{1}{T} \int_{-\frac{1}{2}T}^{\frac{1}{2}T} y(t)dt$$

Carrying out the integration,

$$\overline{y(t)} = 0 .$$

Next, the RMS equation is derived and is

$$\Delta y_{RMS} = \sqrt{\overline{y^2(t)}} = \sqrt{\frac{1}{T} \int_{-\frac{1}{2}T}^{\frac{1}{2}T} y^2(t)dt} .$$

For T=1,

$$\Delta y_{RMS} = \sqrt{\frac{1}{12} + \frac{1}{(2\pi f_c)^2} - \frac{1}{4\pi f_c} \frac{(1+e^{-2\pi f_c})}{(1-e^{-2\pi f_c})}} .$$

Since $\overline{y(t)} = 0$,

$\Delta y_{RMS} = y_\sigma$ (standard deviation about the mean), and

$$y_\sigma = \sqrt{\frac{1}{12} + \frac{1}{(2\pi f_c)^2} - \frac{1}{4\pi f_c} \frac{(1+e^{-2\pi f_c})}{(1-e^{-2\pi f_c})}} .$$

Let us now direct our attention to the rate of change of phase and frequency. Note,

$$f(t) = \dot{y}(t) .$$

Carrying out the differentiation,

$$f(t) = 1 - 2\pi f_c \, e^{-2\pi f_c t} \left(\frac{e^{-\pi f_c}}{1-e^{-2\pi f_c}} \right) .$$

This equation has a minimum at the left boundary and a maximum at the right boundary. Thus,

$$\Delta f_{max} = f(1/2) - f(-1/2)$$

Carrying out the computation,

$$\Delta f_{max} = 2\pi f_c \ .$$

In addition, the frequency slew is computed by differentiating the frequency equation

$$s(t) = \dot{f}(t) \ .$$

Carrying out the differentiation,

$$s(t) = (2\pi f_c)^2 \ e^{-2\pi f_c t} \left(\frac{e^{-\pi f_c}}{1-e^{-2\pi f_c}} \right) .$$

The major difficulty in analyzing the effects of a smoothing loop on waiting-time jitter is the complexity of analytically expressing the variable waiting-time jitter waveform. The frequency content of the waiting time jitter is governed by the stuffing rate and the stuffing opportunity rate. It is a function of the beat between the two rates as well as subharmonics of this beat frequency. A comprehensive analytical effort to define the waiting-time jitter spectrum as part of a spectrum analysis effort is found in the literature (Ref. 2).. To best utilize this study's resources, the decision was made to employ software simulation methods in the analysis.

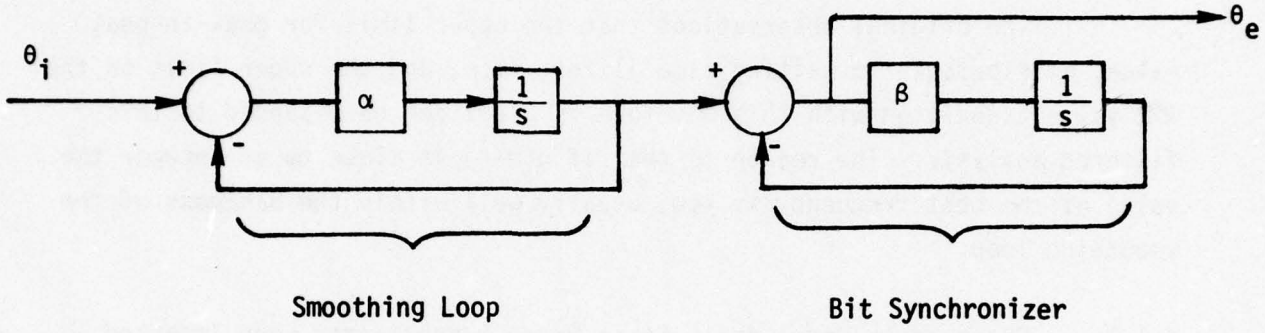
The original observations that the upper limit for peak-to-peak value, attributable to waiting time jitter, is ρ, and the upper limit on the RMS value associated with this waveform is $\rho/\sqrt{12}$ can be expanded to this filtered analysis. The reason is that if $n(n=\frac{1}{\rho})$ is close to an integer the value of the beat frequency is low, usually well within the bandpass of the smoothing loop.

4.1.3 Phase Error Model for a First Order Synchronizer Loop Impacted by a Jittered Input

The problem of integrating the 2nd level pulse stuffing multiplexers into a system which contains modems or bit synchronizers revolves around the effect that the distributary channel output jitter has on their bit timing recovery circuits. Excessive error or high frequency variations can possibly cause a bit sync to lose lock or slip a bit. Even if the jitter is not so severe that the bit timing cannot be recovered, the timing circuits must be compatible with the multiplexer smoothing filter. Since the bit synchronizer output timing is used to make bit decisions, it is not enough that the bit sync track the average input timing. It must track the instantaneous bit timing or the data decisions will be made with a timing error. With matched filter demodulation of unfiltered NRZ data, a timing error of 0.25 bits corresponds to a 6 dB loss in signal-to-noise ratio and a timing error of 0.1 bits corresponds to a 1.9 dB loss in signal-to-noise ratio. The ability of the input bit synchronizer to track input jitter is improved by opening up its loop bandwidth but this impacts the effect of noise on the bit timing recovery so that it is imperative that the bit sync bandwidth be no greater than necessary for proper data demodulation.

It is therefore obvious from the preceding discussion that the tolerance on jitter is dictated by the bit synchronizers that must be made operational with the multiplexer. With this in mind, the analysis effort was subsequently directed at phase error models for synchronizers impacted by jittered inputs.

The first effort addressed a first order bit synchronizer loop. A block diagram of a cascaded first order smoothing loop and first order bit synchronizer is shown in Figure 4.1.3.



$\alpha = 2\pi f_c$

$\beta = 2\pi k f_c$

$k = \beta/\alpha$

Figure 4.1.3. First Order Smoothing Loop and First Order Bit Synchronizer Block Diagram

The transfer function of this cascade from input signal to bit sync phase detector output is

$$H(\omega) = \frac{2\pi f_c}{2\pi f_c + (j\omega)} \cdot \frac{(j\omega)}{2\pi k f_c + (j\omega)} = \frac{2\pi f_c (j\omega)}{[2\pi f_c + j\omega][2\pi k f_c + (j\omega)]} \quad .$$

Expanding this expression into partial fractions (defined for $k \neq 1$),

$$H(\omega) = \frac{1}{(1-k)} \left[\frac{2\pi f_c}{2\pi f_c + j\omega} - \frac{2\pi k f_c}{2\pi k f_c + j\omega} \right] .$$

This expression is the linear sum of two first order loop expressions. Using the results obtained when convolving a first order smoothing loop with a periodic sawtooth waveform representing the unfiltered stuffing jitter, we arrive at

$$\theta_e(t) = \frac{1}{2\pi k f_c} + \frac{1}{1-k} \left(e^{-2\pi f_c t} \cdot \frac{e^{-\pi f_c}}{1-e^{-2\pi f_c}} - e^{-2\pi k f_c t} \cdot \frac{e^{-\pi k f_c}}{1-e^{-2\pi k f_c}} \right).$$

This is the expression for phase error over one stuffing jitter period, $-0.5<t<0.5$. This waveform has a maximum value at the extremes ($t=\pm 0.5$) and a minimum point in-between. The minimum point is located at

$$t = -\tfrac{1}{2} - \frac{1}{2\pi f_c (1-k)} \ln \left(k \cdot \frac{1-e^{-2\pi f_c}}{1-e^{-2\pi k f_c}} \right) .$$

Using this value, the peak-to-peak phase error is expressed as

$$\Delta\theta_{e_{p-p}} = \frac{1}{1-k} \cdot \frac{1}{1-e^{-2\pi f_c}} \left[1 - \frac{1-e^{-2\pi f_c}}{1-e^{-2\pi k f_c}} + \left(\frac{1-k}{k} \right) \cdot \left(k \cdot \frac{1-e^{-2\pi f_c}}{1-e^{-2\pi f_c k}} \right)^{\frac{1}{1-k}} \right] .$$

Additional analysis on the impact of waiting-time jitter was relegated to the software simulator.

4.1.4 Smoothed Output Jitter Models for Second Order Loop

The analysis effort proceeded to study the effect of using a second order smoothing loop on the output jitter. The difference between a first order loop and a second order loop lies in the loop filter. A typical phase locked loop is shown in Figure 4.1.4.

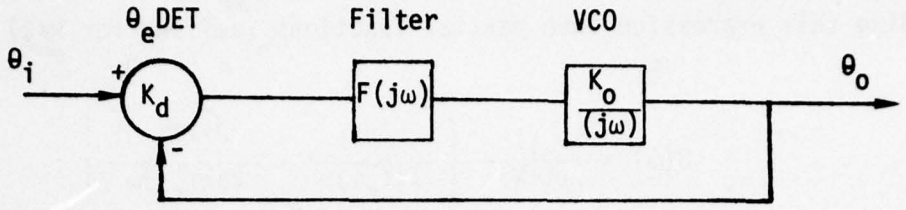


Figure 4.1.4. Basic Loop Block Diagram

The basic loop equation is

$$H(\omega) = \frac{K_o K_d F(j\omega)}{K_o K_d F(j\omega)+j\omega} .$$

A first order loop does not have a filter, it simply has a gain constant

$$F(j\omega) = \alpha .$$

Its transfer function, as stated previously, is

$$H(\omega) = \frac{\omega_c}{\omega_c+j\omega} , \text{ where } \omega_c = K_o K_d \alpha = 2\pi f_c .$$

The filter considered for the second order loop was the form $F(s) = \frac{s\tau_2+1}{s\tau_1}$.
This results in the transfer function for a second order loop

$$H(j\omega) = \frac{2\zeta\omega_n(j\omega)+\omega_n^2}{(j\omega)^2+2\zeta\omega_n(j\omega)+\omega_n^2} .$$

This equation can be written as

$$H(j\omega) = \frac{1}{\alpha-\beta}\left[\frac{\alpha^2}{\alpha+j\omega} - \frac{\beta^2}{\beta+j\omega}\right],$$

where $\alpha\beta=\omega_n^2$ and $\alpha+\beta=2\zeta\omega_n^2$.

The above expression is the linear sum of two first order loop expressions. Using the results obtained when convolving a first order smoothing loop with the periodic sawtooth waveform representing the unfiltered stuffing jitter, the following equation is derived.

$$y(t) = t + \frac{1}{\alpha-\beta}\left[\frac{\alpha e^{-\alpha/2}e^{-\alpha t}}{1-e^{-\alpha}} - \frac{\beta e^{-\beta/2}e^{-\beta t}}{1-e^{-\beta}}\right].$$

Continuing with the exercise, the RMS equation is derived next

$$\Delta y_{RMS} = \sqrt{\overline{y^2(t)}} = \sqrt{\frac{1}{T}\int_{-\frac{1}{2}T}^{\frac{1}{2}T} y^2(t)dt}, \text{ where } T=1.$$

$$\Delta y_{RMS} = \sqrt{\frac{1}{12} + \frac{2}{\alpha\beta} - \frac{1+e^{-\alpha}}{1-e^{-\alpha}}\,\frac{2\beta+\alpha}{1(\alpha^2-\beta^2)} + \frac{1+e^{-\beta}}{1-e^{-\beta}}\,\frac{2\alpha+\beta}{2(\alpha^2-\beta^2)}}.$$

The rate of change of phase and frequency is derived.

$$f(t) = \dot{y}(t), \text{ and}$$

$$f(t) = 1 + \frac{1}{\alpha-\beta}\left[\frac{\beta^2 e^{-\beta/2}e^{-\beta t}}{1-e^{-\beta}} - \frac{\alpha^2 e^{-\alpha/2}e^{-\alpha t}}{1-e^{-\alpha}}\right].$$

In addition, the frequency slew is computed by differentiating the frequency equation, Therefore,

$$s(t) = \dot{f}(t), \text{ and}$$

$$s(t) = \frac{1}{\alpha-\beta}\left[\frac{\alpha^3 e^{-\alpha/2} e^{-\alpha t}}{1-e^{-\alpha}} - \frac{\beta^3 e^{-\beta/2} e^{-\beta t}}{1-e^{-\beta}}\right] .$$

The peak-to-peak phase jitter equation was not obtained because a closed-formed solution for the minimum value of time cannot be derived. The task was continued in the software simulator effort.

4.1.5 Comparison of Smoothing Filter Capabilities Between First Order and Second Order Loops

In considering tradeoffs between a first order smoothing loop and second order smoothing loop, it becomes necessary to compare the filtering characteristics of both. The equations for the two loops (Ref. 11) are the following:

First Order Loop

$$H(j\omega) = \frac{\omega_c}{\omega_c + j\omega} = \frac{1}{1+j\left(\frac{\omega}{\omega_c}\right)}$$

Second Order Loop

$$H(j\omega) = \frac{2\zeta\omega_n(j\omega)+\omega_n^2}{(j\omega)^2+2\zeta\omega_n(j\omega)+\omega_n^2} = \frac{1+j2\zeta\left(\frac{\omega}{\omega_n}\right)}{\left[1-\left(\frac{\omega}{\omega_n}\right)^2\right]+j2\zeta\left(\frac{\omega}{\omega_n}\right)}$$

Note that the function is operating on phase input, and bear in mind that the loops perform a low pass filtering operation on phase input.

Figure 4.1.5-1 shows the filtering characteristics of both loops. The filtering characteristics of a first order loop are not discernible from a second-order with $\zeta=5$ and $\omega_n=(1/10.1)\omega_c$. In addition, the second order loop with a small value of damping constant, ζ, can introduce enhancement of jitter in certain frequency bands.

The relationship for 3 dB bandwidth as a function of the second order loop's damping factor, ζ, and natural frequency, ω_n, is

$$\omega_{3\ dB} = \omega_n \sqrt{2\zeta^2+1+\sqrt{(2\zeta^2+1)^2+1}} .$$

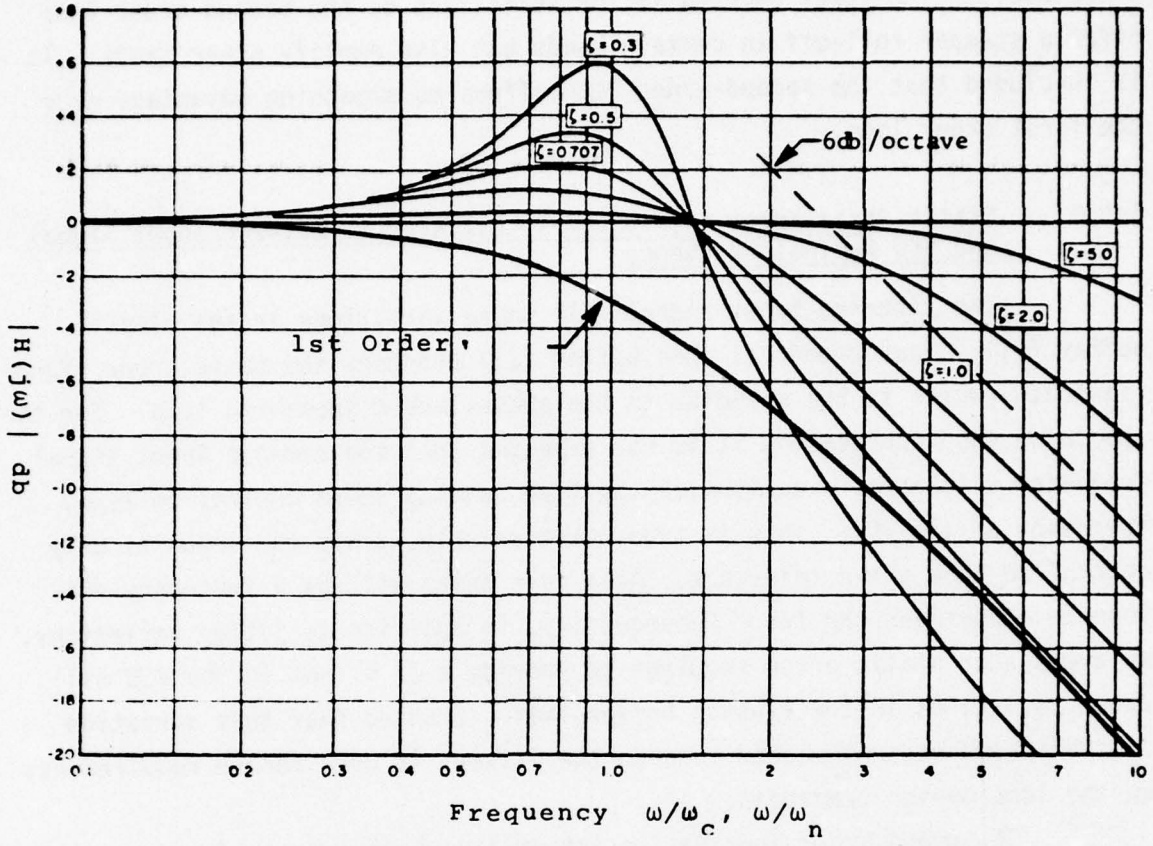


Figure 4.1.5-1. Frequency Response Comparison;
First-Order Loop and High-Gain Second-Order Loop

Figure 4.1.5-2 shows this relationship. Both smoothing loops roll-off at 6 dB/octave. The lower damping factor selections on the second-order loop offer a steeper roll-off in certain bands but also amplify other bands. It is concluded that the second-order loop offers no smoothing advantage over the first order loop.

4.1.6 Static Phase Error Attributed to Differences Between Input Signal and VCO Nominal Frequency

The jittered input signal will cause variations in the elastic buffer fill. Measurement of this buffer fill produces the phase error signal (sawtooth) which is the stimulus to the phase-locked smoothing loop. For the smoothing loop application it is not expected that the average input signal frequency will agree exactly with the free running (zero control voltage) frequency of the VCO. This is true, particularly, since the input is only controlled to a given tolerance. As a rule there will be a frequency difference Δt between the two. Consequently, in addition to jitter variations, an average or static error required to provide a Δf offset in the VCO will cause variations in the elastic buffer fill. Granted that this variation is static and does not contribute to the jitter; it does impose requirements on the loop design tradeoffs.

A second order loop has an integrator which acts as frequency memory. Frequency difference, Δf, is stored in the form of charge on this integrator. Therefore, no error voltage is required to directly maintain this average Δf offset in the VCO. There are two methods for implementation of analog loop filters as discussed in the literature (Ref. 11): passive filters and active filters. For a passive filter the gain is unity so the memory evaporates (discharges) fairly quickly. However, in an active filter it is not difficult to make the gain large so that the error signal is no more than a few degrees for the maximum Δf encountered. For a second order loop the static error can be made minimal by design. In a digital loop implementation this Δf information is stored in a data register. Its not volatile like the analog techniques.

The first order loop has no frequency memory, consequently, the frequency difference Δf must be achieved by maintaining a static phase error. From the equations of the first order loop the phase error required to maintain this Δf is

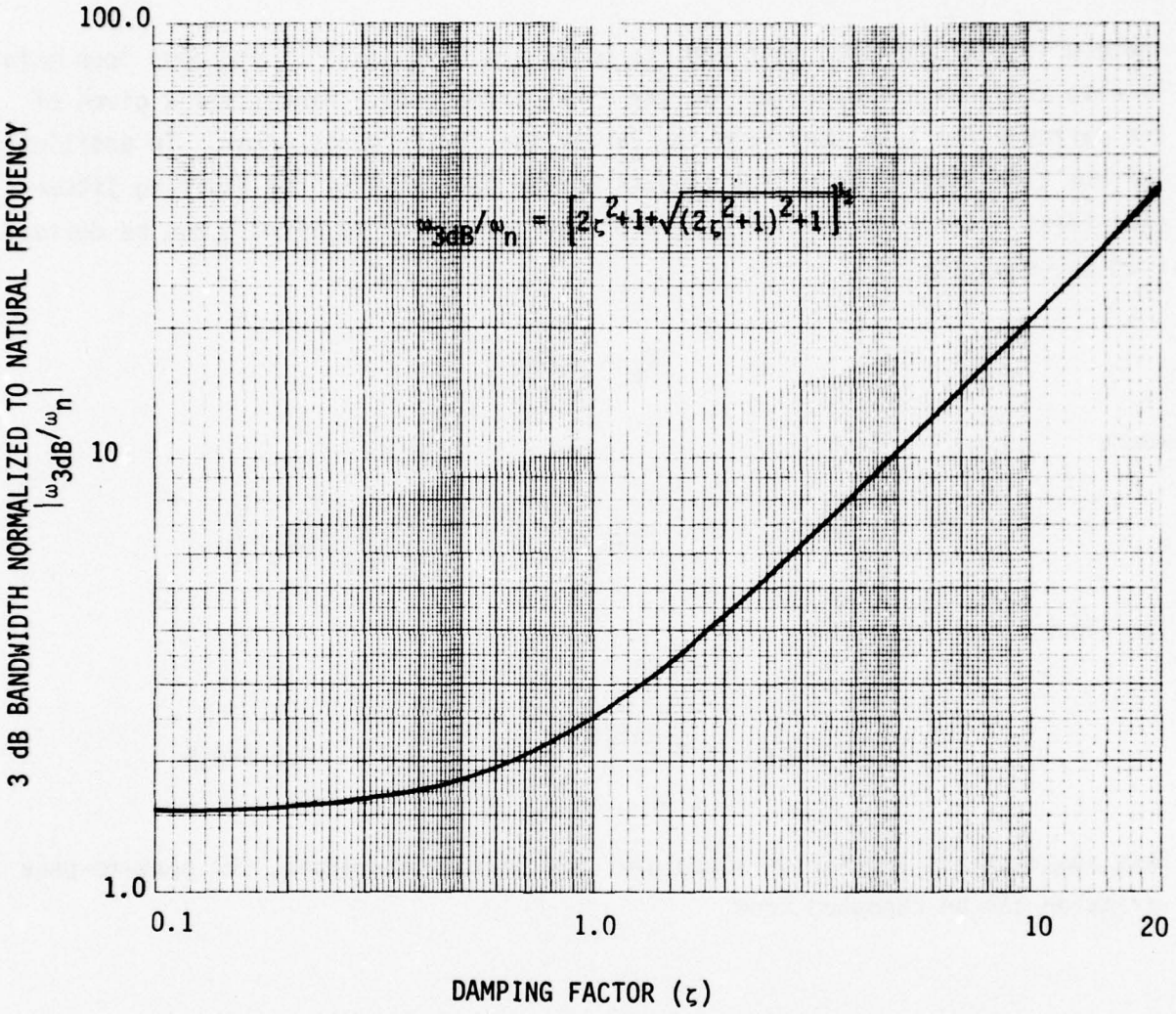


Figure 4.1.5-2. Normalized 3 dB Bandwidth Frequency Versus Damping Factor

$$\theta_e = \frac{2\pi\Delta f}{\alpha} ,$$

where α is the open loop gain and its units are $(\text{seconds})^{-1}$. The open loop gain α is also the loop bandwidth ω_c for the first order loop. Hence, for a given Δf the narrower the loop bandwidth the larger the static phase error. In addition, for the time variations on the elastic buffer generated by the stuffing jitter of a first order loop, a time waveform over one period $-0.5<t<0.5$ can be derived from the equation

$$\theta_e = \theta_i - \theta_o ,$$

where

$$\theta_i = t \text{ and } \theta_o = t - \frac{1}{2\pi f_c} + e^{-2\pi f_c t}\left(\frac{e^{-\pi f_c}}{1-e^{-2\pi f_c}}\right).$$

Therefore,

$$\theta_e(t) = \frac{1}{2\pi f_c} - e^{-2\pi f_c t}\left(\frac{e^{-\pi f_c}}{1-e^{-\pi f_c}}\right). \qquad -0.5<t<0.5$$

This equation has a positive slope over the period, therefore, the peak-to-peak variation can be computed from

$$\theta_{e_{p-p}} = \theta_e(0.5) - \theta_e(-0.5) .$$

This will yield an equation which is intuitive,

$$\theta_{e_{p-p}} = 1 \text{ bit},$$

and is independent of any parameters. It is observed that the lower bound of θ_e ranges over -1.0 bit $\leq$ lower bound $\theta_e \leq$ -0.5 bit, and the upper bound ranges over

0 bit $\leq$ upper bound $\theta_e \leq 0.5$ bit as f_c is varied from $\infty \rightarrow 0$. This range varaition is attributed to the normalization and the fact that the output cannot precede the input.

4.1.7 Audio Channel Performance

This preliminary analysis was initially conducted to determine the effect of pulse stuffing multiplexer jitter on voice quality. As a result of this analysis, it was concluded that the impact would be minimal and a subsequent decision was made to concentrate on bit slip problems. The analysis was done on the HY-12.

The wideband PCM Trunk Carrier Equipment, HY-12, is an 8 bit μ law companded digitizer and channel multiplexer. In the TSEC/CY-104 configuration the timing to the HY-12 is supplied by the HN-74. Thus, timing jitter is not an equipment problem of the HY-12. However, the audio waveforms for each channel are reconstructed in this device so that timing degradations on the signals must be considered.

The timing degradation should be compared to other distortion effects to determine its impact. Some of these effects are quantization error, bit error effects, interpolation distortion, envelope delay, and frequency response. The output signal-to-noise ratio caused by quantizing noise and bit errors is shown in Figure 4.1.7-1 as a function of the full scale loading of the A/D converter. Folded binary coding with an 8 bit compander, μ=255, is used.

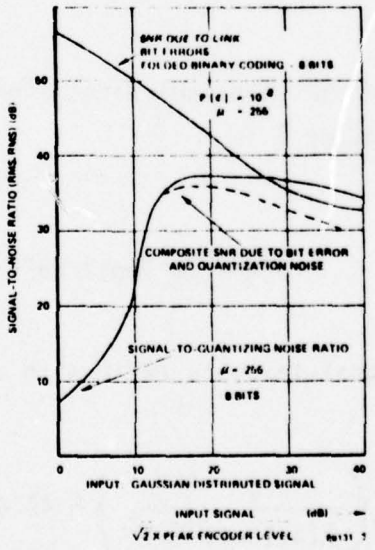


Figure 4.1.7-1. Curves Plotting Performance Data for the HY-12

The peak SNR available is 36 dB. The frequency response of the transmit (pre-sampling) filter in the HY-12 is given in Figure 4.1.7-2 and of the reconstruction (interpolation) filter in Figure 4.1.7-3. The transmit filter prevents an increase of noise folded into the passband. For 3.5 kHz bandwidth this effect is greater than 40 dB down. The reconstruction filter is used to remove the voice channel image centered at 8 kHz. The peak out-of-band response of this filter is approximately 22 dB down, which could cause some degradation of the signal-to-noise ratio. However, audio headsets or another interpolation filter cascaded with this one can improve the signal-to-noise ratio such that interpolation effects are negligible.

For minimal effect, timing jitter contribution to the channel performance should be maintained at a level of 46 dB or more below the signal. This would affect overall signal-to-noise ratio by less than 0.5 dB.

It is not anticipated that a moderate amount of jitter will seriously degrade voice quality. This conclusion is based on the following calculations of test tone to noise ratio with desynchronizer jitter.

Let the RMS jitter on a T1 carrier be x bits. This corresponds to a time jitter of x/1.544 μs. If this amount of jitter is present on a 1020 Hz test tone, then the phase jitter in radians is

$$2\pi \frac{x/1.544}{1/0.001020} = 4.15 \times 10^{-3} \times \text{rad.}$$

It is well known that the equivalent signal-to-noise ratio of a sinusoid with RMS phase jitter θ is

$$S/N = 10 \log(1/2\theta^2)$$

so that the equivalent signal-to-noise ratio with x bits of T1 multiplexer jitter is

$$S/N = 10 \log \left(\frac{1}{2(4.15 \times 10^{-3} x)^2} \right) = 44.6 - 20 \log x \text{ dB} .$$

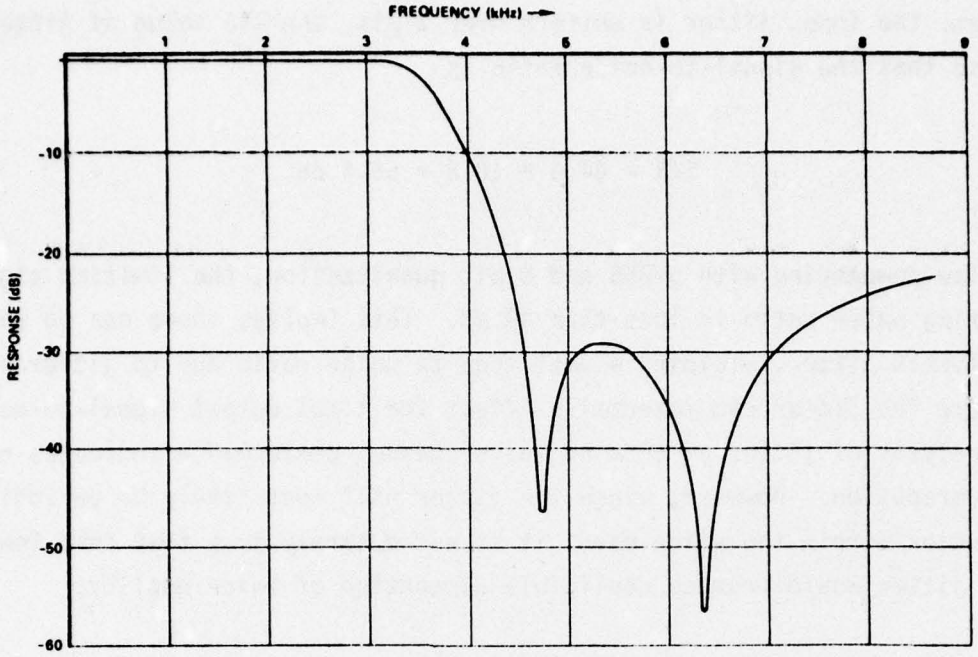


Figure 4.1.7-2. Transmit-Filter Response of HY-12 Frequency (kHz)

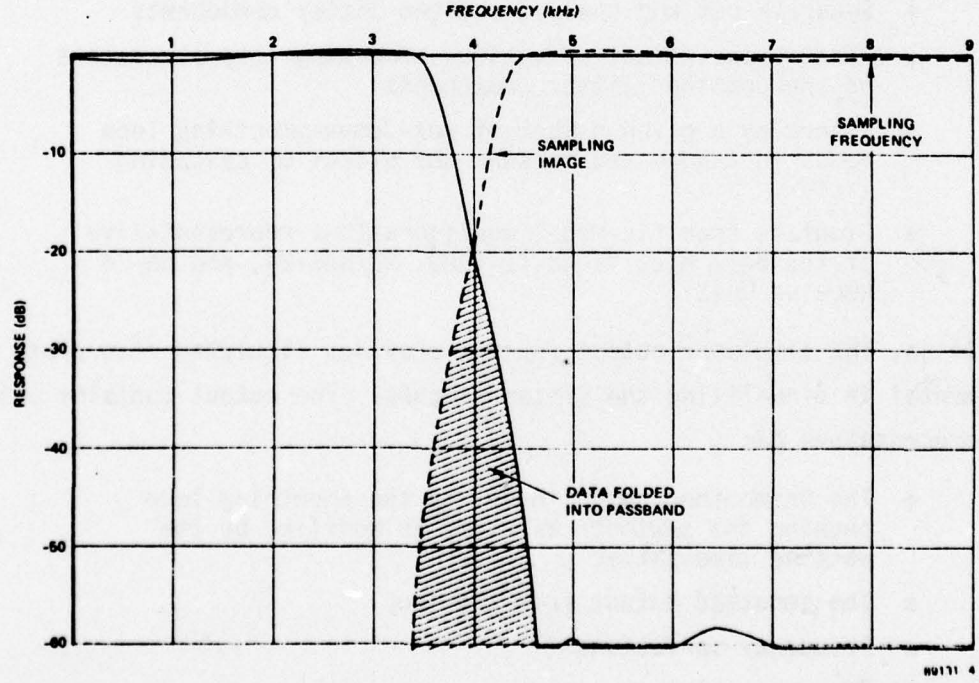


Figure 4.1.7-3. Reconstruction Filter Response of HY-12

If, then, the input jitter is uniform over 1 bit, the RMS value of jitter is $1/\sqrt{12}$ so that the signal-to-noise ratio is

$$S/N = 44.6 + 10.8 = 55.4 \text{ dB}.$$

For μ law companding with μ=255 and 8 bit quantization, the limiting signal to quantizing noise ratio is less than 40 dB. This implies there can be up to 10 bits of peak jitter, yielding a test tone to noise ratio due to jitter of 45.4 dB before the jitter can materially affect the total output signal-to-noise ratio. This analysis of jitter effects on voice channel performance indicates no significant degradation. However, since the jitter will most likely be periodic at frequencies within the voice band, it is not entirely true that this low value of jitter would produce negligible distortion of voice quality.

4.2 Software Simulator Approach

The requirement for the software simulator was generated from a need to extend the analysis effort. The software simulator provides a tool to:

- Separate out and analyze the two jitter components
- Measure the effect of various smoothing loop parameters on the combined jitter components
- Interplay a given number of mux-demux-smoothing loop nodes in tandem and measure the effect of cascading jitter
- Simulate specific model configurations representative of the Bell M12, VICOM T1-4000, AN/GSC-24, and HN-74 Receive Unit

In addition, the simulator output routine provides simulated time plots which are instrumental in visualizing the jitter process. The output contains plots which are representative of:

- The unsmoothed output prior to the smoothing loop showing the sawtooth waveform as modified by the waiting time jitter
- The smoothed output from the loop
- Frequency variations
- Frequency slew variations
- Tracking error on the bit synchronizer

The simulator in addition collects statistics and provides summary reports on peak-to-peak and RMS values for phase jitter, frequency variations, frequency slew variations, and tracking error. In addition, it has the capability of providing histograms for the above variables.

The simulator (MUXJIT) is written in GASP IV, a FORTRAN based simulation language (Ref. 12). It takes advantage of the GASP IV Combined Simulation features which allow the simulation of variable discrete time events representative of pulse stuffing requirements along with the continuous simulation required for the waveforms of input jitter, output jitter, phase error, etc.

Definition of the simulator model was done concurrently with that of the analysis model. The prime task is the definition of the four parameters of the simulator: Input, output, variables of simulation, and implementation mechanism. The results of these tasks are summarized in Figure 4.2. A principal feature of the software simulator is the ability to take the jittered output of a node and make that the input to another node. This allows the simulation of cascaded nodes. A detailed description of the model and simulator including a program listing is contained in Appendix B.

4.3 Hardware Test Bed Approach

The hardware simulator was a requirement of the statement of work. There are several reasons for developing a test bed:

- Gives the study the necessary hardware depth. Often times analysis overlooks implementation difficulties, the hardware approach forces the analysis to study the implementation problems.
- Verifies the analysis and software simulator results. Assumptions made in modelling can conceivably invalidate the results. The test bed is a step closer to fielded hardware.
- Overcomes the limitations of the other approaches. Waiting-time jitter and cascade jitter were difficult to analyze. The software simulator compensated for this deficiency, but it has run time and spectrum analysis limitations.
- Provides a hardware vantage point. A key requirment in analyzing a problem is to understand the problem. The availability of such a simulator contributes another point of view to further the understanding.

VARIABLES OF SIMULATION

DATA TRANSPORT (T2) RATE

ρ, STUFFING RATIO

N, NUMBER OF CASCADED NODES

PHASE OFFSET BETWEEN CASCADE NODES

ORDER AND PARAMETERS OF SMOOTHING LOOP

ORDER AND PARAMETERS OF BIT SYNCHRONIZER

GENERAL INPUTS

TRIBUTARY CHANNEL (T1) RATE

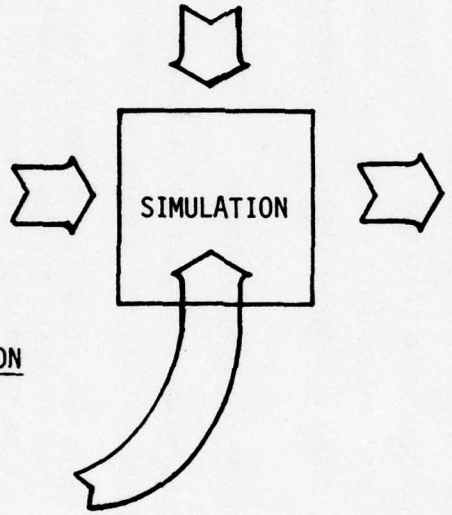
VCO NOMINAL FREQUENCY FOR EACH NODE

SOFTWARE SIMULATOR IMPLEMENTATION

FORTRAN

GASP IV

DATACRAFT HOST



OUTPUTS OF SIMULATION EXPERIMENT

MEASURE OF "WAITING-TIME" JITTER

MEASURE OF "CASCADE" JITTER

MEASURE OF LOOP-ORDER ON JITTER

MEASURE OF LOOP PARAMETERS ON JITTER

MEASURE OF BUFFER SIZE REQUIREMENTS

MEASURE OF FREQUENCY/FREQUENCY SLEW

MEASURE OF JITTER EFFECT ON BIT SYNCHRONIZER ERROR

FIGURE 4.2. MUXJIT SIMULATOR OPERATION

- Provides tandeming capability with fielded equipment. Although interface modifications might be required, the flexibility of this capability will allow the exercising and testing of field equipment to obtain information not available from modelling exercises.

The test bed approach, labeled the Second Level Multiplexer Simulator (SLMS), provides three sets of jitter simulator and smoothing loop functions. The three sets permit deriving results for cascading jitter. The SLMS was constructed in a rack mounted chassis, and the mechanical design is a standard rack mount packaging which is ruggedized to standard lab operation. This design is intended for portability between facilities. A complete description of the hardware test bed simulator design is contained in "Design Plan for Pulse Stuffing TDM Network Study," a companion document (Ref. 13). This document contains a complete description of the SLMS in that it covers its development from design tradeoffs to schematic diagrams.

In addition, "Test Plan for Pulse Stuffing TDM Network Study," another companion document (Ref. 14) describes the experiments which will be accomplished with the SLMS during Phase II. This document amplifies on the capability of the SLMS.

A result of using the hardware simulator is that a portion of the study has been directed to investigating instrumentation methods. Several ideas for Jitter Test Sets to verify compliance with specifications have been generated. These ideas stem from the requirements to measure peak-to-peak jitter and RMS jitter using the concept of obtaining time waveform snapshots. A phase detector/oscilloscope combination will be used to derive snapshots for the tests in Phase II.

SECTION 5.0

DESIGN CHARACTERISTICS OF PULSE STUFFING MULTIPLEXER NETWORK SYSTEMS

5.0 DESIGN CHARACTERISTICS OF PULSE STUFFING MULTIPLEXER NETWORK SYSTEMS

The prime objective of this study is to provide knowledge of the performance of networks utilizing pulse stuffing second level multiplexers. Prior sections have discussed the groundwork that was layed to elicit this knowledge. This section discusses the results to date. These results were obtained from the analysis and software efforts; findings from the hardware simulator effort will be included in the final report.

In designing a pulse stuffing multiplexer network system, normally, the following parameters are fixed by the application:

- Number of nodes
- Tributary channel input rate and tolerance
- VCO nominal frequency (this study only considered single tributary channel input rate systems)
- Bit synchronizer parameters (although a tradeoff could result from jitter vs bandwidth noise considerations)

The following parameters are usually design parameters selected by the system designer:

- Data transport rate (including selection of multiplexer category)
- Number of bits between stuffing opportunities (a function of the overhead bits)
- Smoothing loop order and parameters (including the demultiplex/smoothing loop interface elastic buffer sizing)

The bit synchronizer parameters normally establish the acceptance criteria for jitter tolerance. The selection of multiplexer categories is dramatically impacted by other criteria (i.e., the desire to select a pulse stuffing scheme which is more readily adapted to a synchronizer transmission scheme). For the four pulse stuffing multiplexer schemes described in the literature, the following is a broad sweeping summary of their applications:

- Negative stuffing is not popular
- Positive stuffing has been used successfully but is not directly adaptable to synchronous systems
- Positive-zero-negative stuffing has low frequency stuffing jitter components which are difficult to filter

- Positive-negative stuffing was proposed as an alternative to the low frequency stuffing jitter components. This CCITT recommendation was not studied because of present program resource limitations.

The first-order smoothing loop has a minimum bandwidth limitation imposed by a combination of phase detector operating range (elastic buffer size) and the data rate deviation tolerance range of the tributary input channel. A second-order smoothing loop is necessary if a lower bandwidth smoothing loop is needed. However, a second-order loop has the undesirable property of enhancing certain bandwidths, consequently, a judicious compromise of damping ratio (ζ) and natural frequency (ω_n) is needed.

5.1 Output Jitter Characteristics of Second Level Multiplexers

The characteristics of the jitter presented at the output of a pulse stuffing multiplexer have been analyzed with a considerable degree of rigor by several investigators (Ref. 1,2,3). The most comprehensive published analysis of this jitter, including the effects of the smoothing loop and cascaded systems has been presented by Duttweiler. This study effort capitalizes on this work and further expands the investigative areas with a time domain approach in an effort to understand the influencing factors.

Normally, the multiplexers are required to operate over a range (tolerance) of tributary input channel digital rates. This implies that the multiplexer will operate over a range of stuffing ratios since the stuffing ratio is a function of the tributary input channel digital rate, the data transport rate, and the number of bits between stuffing opportunities. The latter two are design parameters, which are selected during system design. The former is a system operating requirement.

The phase jitter waveform caused by the stuffing/destuffing process is a highly complicated function of the pulse stuffing format. This waveform consists of two elements: pulse stuffing jitter and waiting time jitter. The stuffing jitter is a function of the data transport rate and the tributary channel input digital rate. Its amplitude is 1 bit (the stuffed bit), and its rate is the difference of the two rates. The waiting time jitter is, in reality, a modulation of the stuffing jitter brought about because stuffing must be delayed until the next stuffable digit time slot occurs. Its frequency is governed by the stuffing rate and the stuffing opportunity rate. It is a function of the beat

between the two rates as well as subharmonics of this beat frequency. The amplitude ranges from a peak value of ρ (stuffing ratio) bits to 0 bits.

Normally, before the distributary channel output is routed to the output port of the first level demultiplexer, it is filtered by a smoothing loop. The smoothing done on the phase jitter is a function of the smoothing loop bandwidth and the frequency content of the phase jitter. In a positive pulse stuffing multiplexer, the data transport rate can be selected so that the pulse stuffing jitter frequency is high and can be easily filtered. In a positive-zero-negative stuff multiplexer the data transport rate is fixed, usually at midrange of the tributary channel input data rate tolerance. The smoothing loop bandwidth, theoretically, is bound by the slew rate of the tributary input channel data. In practice the bandwidth is limited by the practicality of using a smoothing loop with extremely narrow bandwidths.

The formatted overhead bits control the number of data bits per stuffing opportunity. A larger number of overhead bits is required to lower the number of data bits per stuffing opportunity. For a selected data transport rate, the smaller the number of data bits per stuffing opportunity, the lower the stuffing ratio, ρ, and consequently, the lower the waiting time jitter magnitude. However, the larger number of overhead bits increases the bandwidth requirements. Also the increased number of stuffable time slots increases the probability of error, consequently, decreasing the reliability of operation.

5.1.1 Effects of Varying the Stuffing Ratio

The literature search indicated that Duttweiler (Ref. 2) has the most comprehensive set of results. A reproduction of his Figure 10, shown in Figure 5.1.1-1, demonstrates the effect of varying the tributary input channel data rate for a given second level multiplexer configuration. This theoretical curve is for a specific Bell M12 application with 5368 Hz stuffing rate and a double pole at 322 Hz.

At the lower stuffing ratios, the offset between the data transport rate and the tributary channel input rate was low enough that the smoothing filter was not adequate to significantly attenuate the pulse stuffing jitter component. At a stuffing ratio near 1, the peak-to-peak waiting time jitter is 1 bit and its frequency is low so that the smoothing filter doesn't attenuate

it. Consequently, at a stuffing ratio near 0 or 1, the peak-to-peak jitter is 1 bit so that the RMS value is 10.8 dB below 1 bit. Near $\rho=\frac{1}{2}$, the jitter should be ½ bit or 6 dB below the value at $\rho=1$. Other jitter values near $\rho=1/3$, 1/4, and 1/5 should have peak-to-peak amplitudes of 1/3, 1/4, and 1/5 respectively so that the RMS values should be 9.6, 12 and 14 dB below the RMS value at $\rho=1$. These results derived from the model that the peak-to-peak value of waiting time jitter is equal to ρ are the same results as those shown in Figure 5.1.1-1.

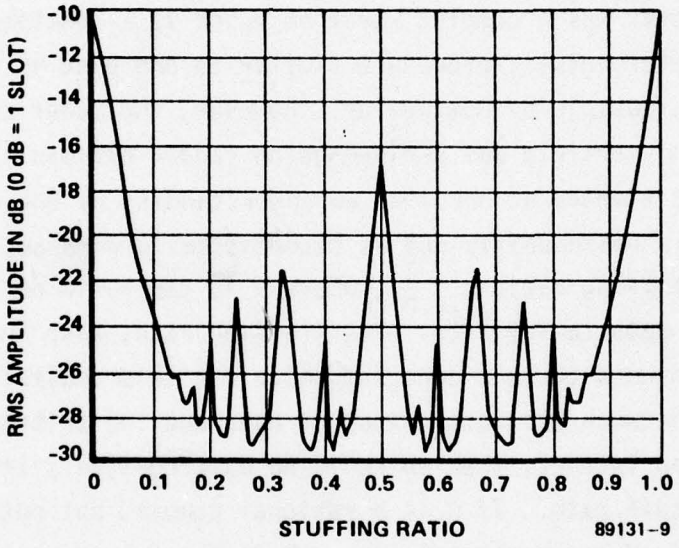


Figure 5.1.1-1. A Theoretical Graph of the RMS Amplitude of Filtered Waiting Time Jitter as a Function of ρ with H(f) Assumed to have a Double Pole at 0.06 Cycle per Stuffing Opportunity

Using the software simulator, MUXJIT, an experiment was conducted which involved varying the number of bits per stuffing opportunity. A postulated VICOM T1-4000 model was used. The data transport rate was 1,544,935 Hz, the tributary channel input rate was 1,544,000 Hz, and the smoothing loop

cutoff frequency was 46.75 Hz. The experiment involved the given set of data bits per stuffing opportunity of 288, 576, 864, and 1152, with a corresponding ρ = .1743, .3486, .5229, and .6972. The results of RMS jitter and peak-to-peak jitter, both in degrees, are shown in Figures 5.1.1-2 and 5.1.1-3, respectively. In this particular experiment the effect of stuffing jitter is held constant; that is, the data rate offset between data transport rate and tributary channel input rate was not varied and neither was the smoothing loop's cutoff frequency. This variation is strictly attributed to waiting time jitter. The results parallel Figure 5.1.1-1; however, such comparisons are limited by the small quantity of data points.

An effort was made to isolate and analyze the elements that affect the waiting-time jitter frequencies. A heuristic approach, based on observations of results from MUXJIT, was pursued. The literature seach stated that waiting time jitter was a complex waveform which is a function of the stuffing ration, ρ. A deterministic procedure similar to one used by Iwerson (Ref. 15) was proposed as feasible by Duttweiler. However, the power spectrum of waiting time jitter in his article was derived using random process theory. The approach pursued here was slanted at deriving an understanding of the cause in a relative short time and is consequently not as mathematically rigorous in nature.

The stuffing ratio $\rho = \frac{1}{n}$, where ρ is the ratio of stuffing rate to the stuffing opportunity rate. The stuffing rate, also known as the offset frequency, is assumed to be a constant value for this analysis. This rate is the difference between the data transport rate and the tributary channel input rate. If n is an integer, then there is no waiting-time jitter and stuffing occurs at the stuff rate. If n is a rational number, but not an integer, then $\rho = \frac{M}{N} = \frac{1}{n}$, where M and N are integers. Defining $[n]$ to represent the greatest integer function of n and setting $m=[n]$, it is noted that the waiting time effect will generate a waveform which consists of stuffs occurring at m or m+1 stuffing opportunities apart.

Letting α = number of periods of m stuffing opportunities in length contained in the sequence.

β = number of periods of m+1 stuffing opportunities in length contained in the sequence.

$$\alpha + \beta = M$$

$$\alpha m + \beta(m+1) = N$$

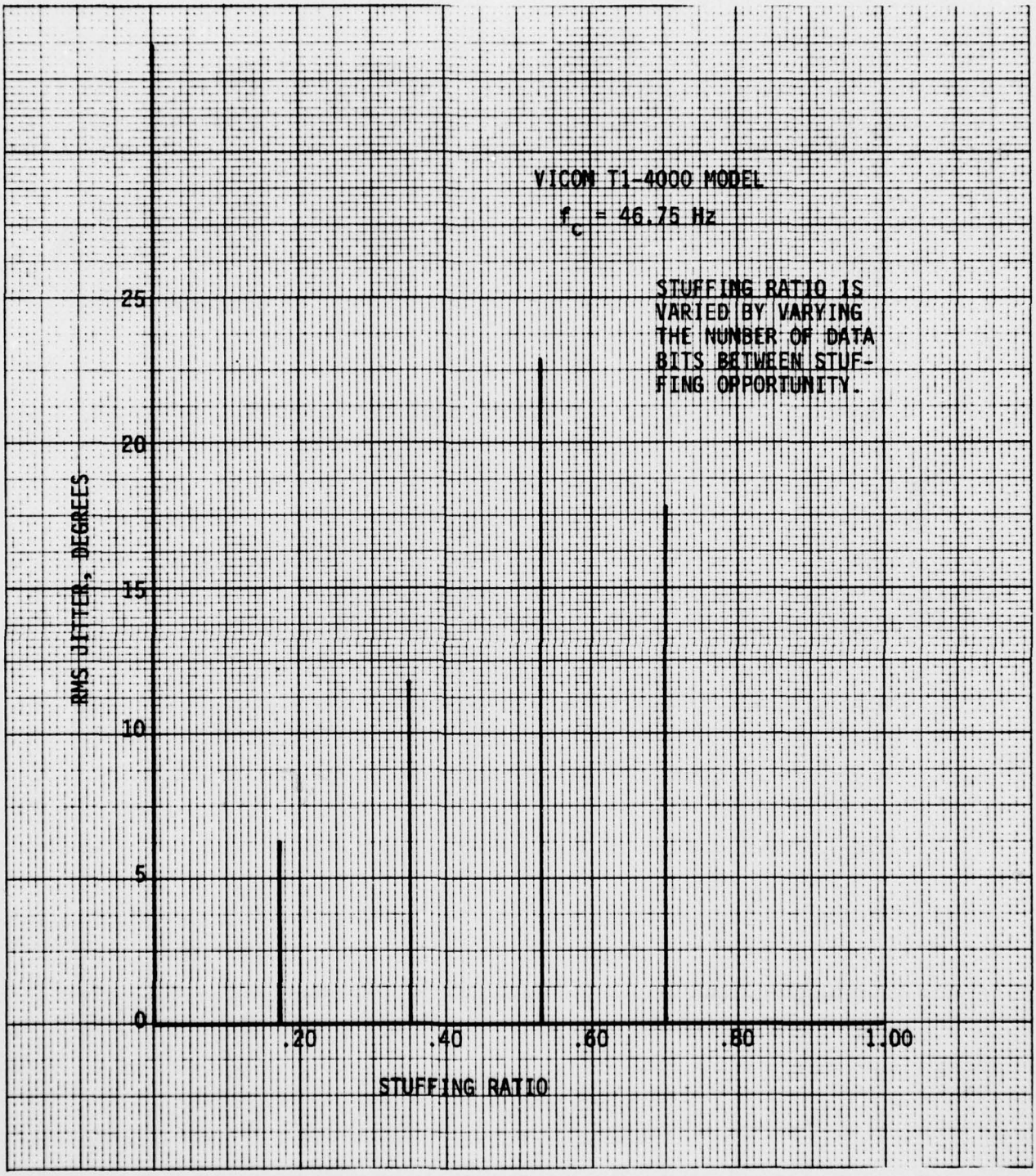


Figure 5.1.1-2. RMS Jitter Versus Stuffing Ratio for the VICOM T1-4000 Parameters and Cutoff Bandwidth of 46.75 Hz

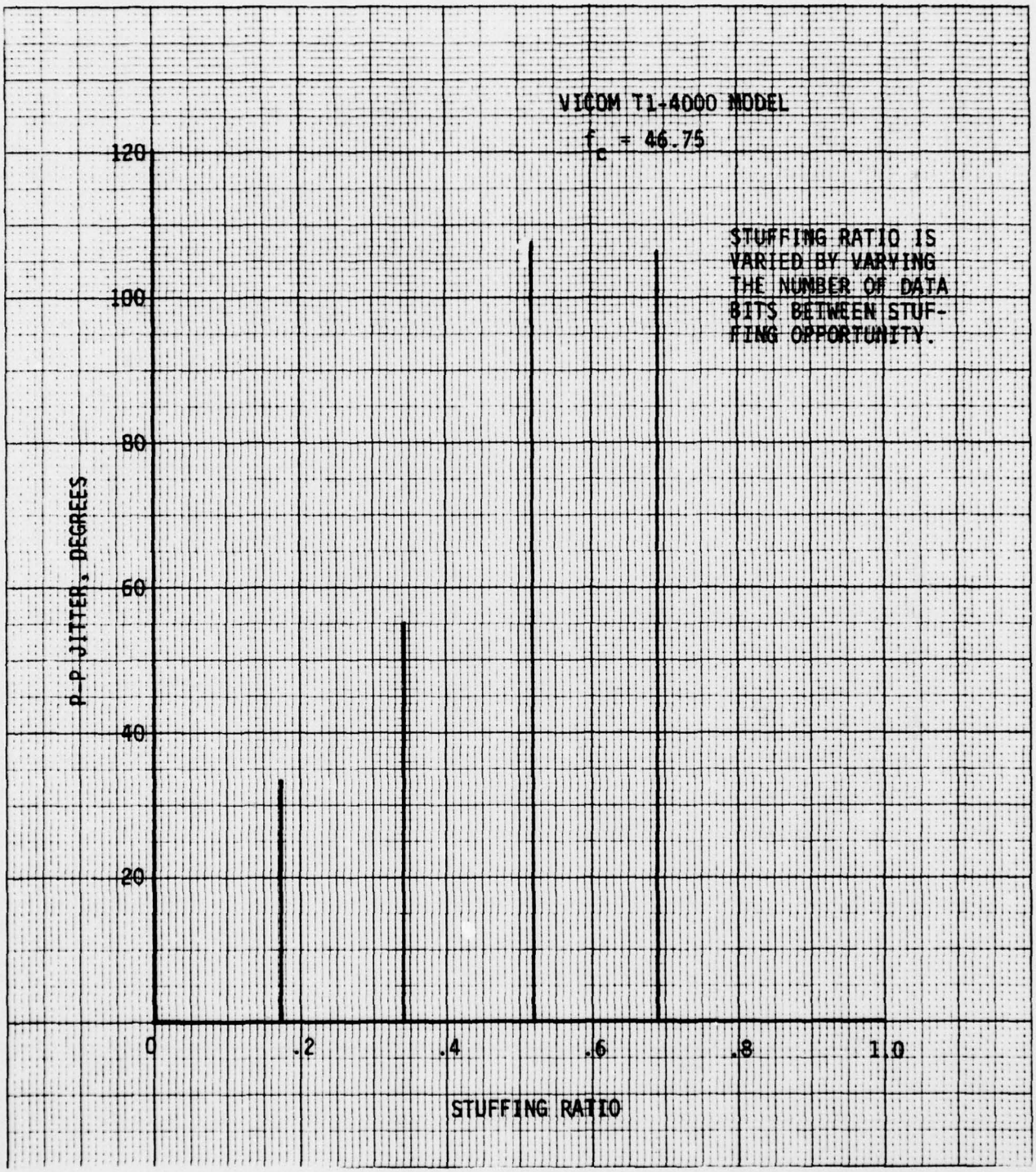


Figure 5.1.1-3. Peak-to-Peak Jitter Versus Stuffing Ratio for the VICOM T1-4000 Parameters and Cutoff Bandwidth of 46.75 Hz

From these expressions the number of m and m+1 periods can be obtained. Note that the overall period is N stuffing opportunities, and M stuffs occur during that period. If n is an irrational number, then there is no overall period. The waiting time effect will generate a waveform which consists of stuffing occuring at m and m+1 stuffing opportunities.

Observation of the waveform patterns provide interesting insight into the various frequencies generated. Table 5.1.1 shows some results of this heuristic investigation of waveforms generated while conducting experiments using MUXJIT. It is pointed out that while the stuffing ratio used in the experiments contained extremely long sequences, the observations were truncated to a proximity stuffing ratio number which yielded a short sequence. This is, of course, attributed to the run time limitation.

In Table 5.1.1 the first three columns show the control parameters for the specific experiment. Column 4 depicts the observed experimental repetitive sequence. This sequence is shown as a sequence of ordered pairs k_1-l_1, k_2-l_2, ... For this designation l is the distance between stuffs stated in number of stuffing opportunities, and k is the number of times that l is repeated before proceeding to the next ordered pair in the sequence. Then the sequence repeats itself. The brace shows the number of subsequences (P) within the sequence. Column 5 shows the measured values M and N, where $M = \sum_{i=1}^{s} k_i$, s=number of ordered pairs in the sequence, $N = \sum_{i=1}^{s} k_i l_i$. Column 6 tabulates the measured ρ and n, where ρ=M/N, and n=1/ρ. Note that this column shows the proximity rational number that was observed during the time-limited run. Column 7 indicates observed frequencies of the sequence events. It is noted that m and m+1 divided into the stuffing opportunity rate (SO RATE shown in column 3) are fundamental frequencies. However, what is listed in column 7 are subharmonics generated by the overall sequence. They are computed from (SO RATE/N), and the subsequent value is computed by P(SO RATE/N). These lower frequencies are considered of interest because they are normally hard to eliminate with the smoothing loop. There are, of course, higher order harmonics of these frequencies occurring in the waveshape. Within the scope of this effort, determination of such was not considered necessary. Also note that other lower frequencies created in essence by the long periodicity of the specific ρ are not available because of the limited run time. In fact, extremely low frequency variations are not considered. This is not a problem because they can be tracked by

Table 5.1.1.

Waiting Time Jitter Frequencies Observed From MUXJIT Results

MODEL	ρ&n	BPO/ SO RATE**	EXPERIMENTAL REPETITIVE SEQUENCES*	MEASURED M/N	MEASURED ρ&n	MEASURED W-T JITTER FREQUENCIES
VICOM	.1743 5.737	288 Bits 5364.4 Hz	3-6,1-5	4/23	.1739 5.75	233.2
VICOM	.3486 2.869	576 Bits 2696.2 Hz	7-3,1-2, 6-3,1-2 } 2	15/43	.3488 2.8667	62.4 124.8
VICOM	.5229 1.912	864 Bits 1788.1 Hz	10-2,1-1, 11-2,1-1 } 2	23/44	.5227 1.913	40.6 81.3
VICOM	.6972 1.434	1152 Bits 1341.1 Hz	1-2,1-1,1-2,1-1,1-2,1-1,1-2,2-1 1-2,1-1,1-2,1-1,1-2,2-1 1-2,1-1,1-2,1-1,1-2,2-1 1-2,1-1,1-2,1-1,1-2,2-1 } 4	30/43	.6977 1.4333	31.2 124.8
BELL	.3346 2.9986	288 Bits 5367.3 Hz	86-3,1-2	87/260	.3346 2.9885	20.6
MARTIN	.2225 4.499	889 Bits 1736.8 Hz	1-5,1-4	2/9	.2222 4.5	193.0
MARTIN	.2118 4.7207	889 Bits 1736.8 Hz	3-5,1-4,3-5,1-4,2-5,1-4 3-5,1-4,2-5,1-4 } 2	18/85	.2118 4.7222	20.4 40.8

*k-l where k is number of times the sequence repeats, l is number of stuffing opportunities in the sequence
**Stuffing Opportunity Rate

the bit synchronizer. It is observed that for a given stuffing ratio ρ and its corresponding n, a constant offset frequency, and $m<n<m+1$, the waveform consists of a combination of stuffs which occur at m or m+1 stuffing opportunities apart. It is further noted that the combination of m length stuffs and m+1 length stuffs are used in a sequence such that

$$n = \frac{\alpha m+\beta(m+1)}{\alpha+\beta} \quad .$$

α = number of m length stuffs
β = number of m+1 length stuffs

That is, they are used a given number of times to produce an average equal to n stuffs. An m+1 stuff always starts the sequence. If $m=n-\varepsilon$ with $\varepsilon\simeq 0$, the sequence contains a large number of m stuffs; if $n=m+1-\varepsilon$ with $\varepsilon\simeq 0$, the sequence contains a large number of m+1 stuffs. Should $n=m+\frac{1}{2}$, the sequence would consist of the alternating sequence, m+1 stuff followed by m stuff. When $n=m+\frac{1}{4}$, the sequence consists of one m+1 stuff followed by three m stuffs; if $n=m+\frac{3}{4}$, then the sequence consists of three m+1 stuffs followed by one m stuff.

It is further noted that for $n<m+\frac{1}{2}$ the sequence will consist of isolated m+1 stuffs; that is, m+1 stuffs are not bunched together but rather they are isolated from each other by m stuffs. m stuffs can be bunched-up; in fact, as $n\to m$ larger grouping of m stuffs appear in a given sequence. Conversely, for $n>m+\frac{1}{2}$, the sequence will consist of isolated m stuffs, and m+1 stuffs can be bunched together. As $n\to m+1$, larger groups of m+1 stuffs appear in the sequence.

In the $n<m+\frac{1}{2}$ case, the sequence has an immediate build-up of jitter when the m+1 stuff occurs. This jitter (phase displacement) is gradually reset during the sequence of m stuffs, until the next m+1 stuff when the jitter is again built up. Note that the reset does not necessarily return the phase displacement to the original value. When this happens, there are subharmonics generated by this sequence. In the $n>m+\frac{1}{2}$ case the sequence gradually builds up and dramatically resets.

Two additional examples to amplify the preceding discussion are given below:

a) GIVEN n=2.01, consequently, ρ=0.4975, m=2, and m+1=3.

In this example M=100 and N=201. This sequence consists of 1-3, 99-2. In essence, it has a rapid buildup of jitter offset and a gradual reset.

b) GIVEN n=2.99, consequently, ρ=0.3344, m=2, and m+1=3.

In this example M=100 and N=299. This sequence consists of 99-3, 1-2. In essence, it has a gradual buildup of jitter offset and a rapid reset.

In summary, the waiting-time jitter is controlled by the functions which make up the stuffing ratio. As the stuffing ratio varies, it changes the frequencies and amplitude of waiting time jitter.

5.1.2 Effects of A Smoothing Loop

Although a portion of waiting time jitter will generally occur at low frequencies so that it cannot be removed by smoothing, the stuffing jitter component, if the offset frequency is of sufficient magnitude, can be significantly attenuated by narrow bandwidth smoothing loops. It is obvious that the narrower the loop bandwidth, the lower the output jitter.

Using a first order loop, the peak-to-peak output stuffing jitter is expressed as:

$$\Delta y_{p-p} = \frac{1}{(1-e^{-2\pi f_c})} - \frac{1}{2\pi f_c}\left[1+\ln\left(\frac{2\pi f_c}{1-e^{-2\pi f_c}}\right)\right],$$

and the RMS output stuffing jitter is expressed as

$$\Delta y_{RMS} = \sqrt{\frac{1}{12} + \frac{1}{(2\pi f_c)^2} - \frac{1}{4\pi f_c} \cdot \frac{(1+e^{-2\pi f_c})}{(1-e^{-2\pi f_c})}} \quad .$$

The effect of f_c, the smoothing loop bandwidth normalized to stuffing rate, on peak-to-peak stuffing jitter is shown in Figure 5.1.2-1 and on RMS stuffing jitter in Figure 5.1.2-2.

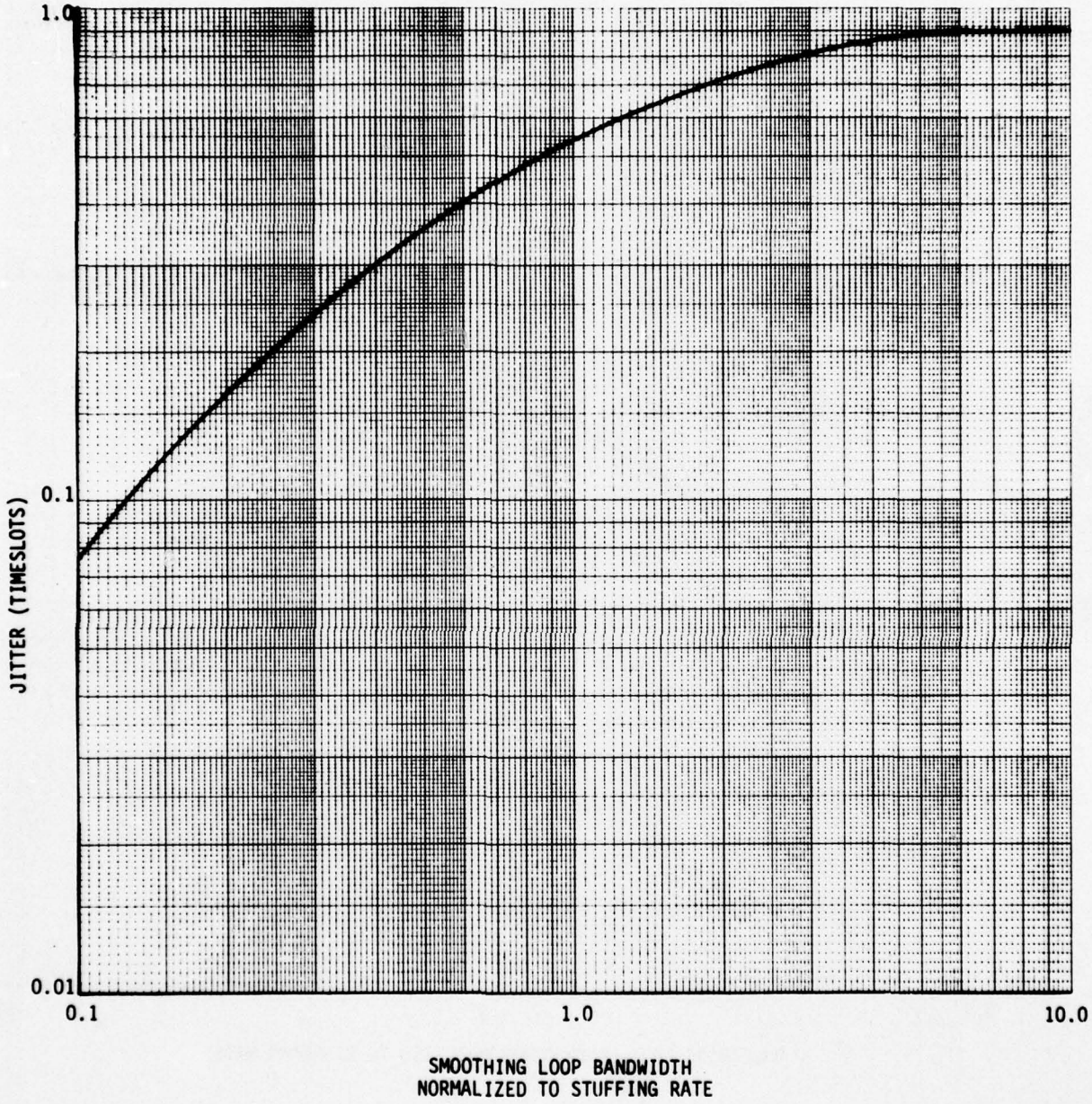


Figure 5.1.2-1. Peak-to-Peak Jitter at First Order Smoothing Loop Output

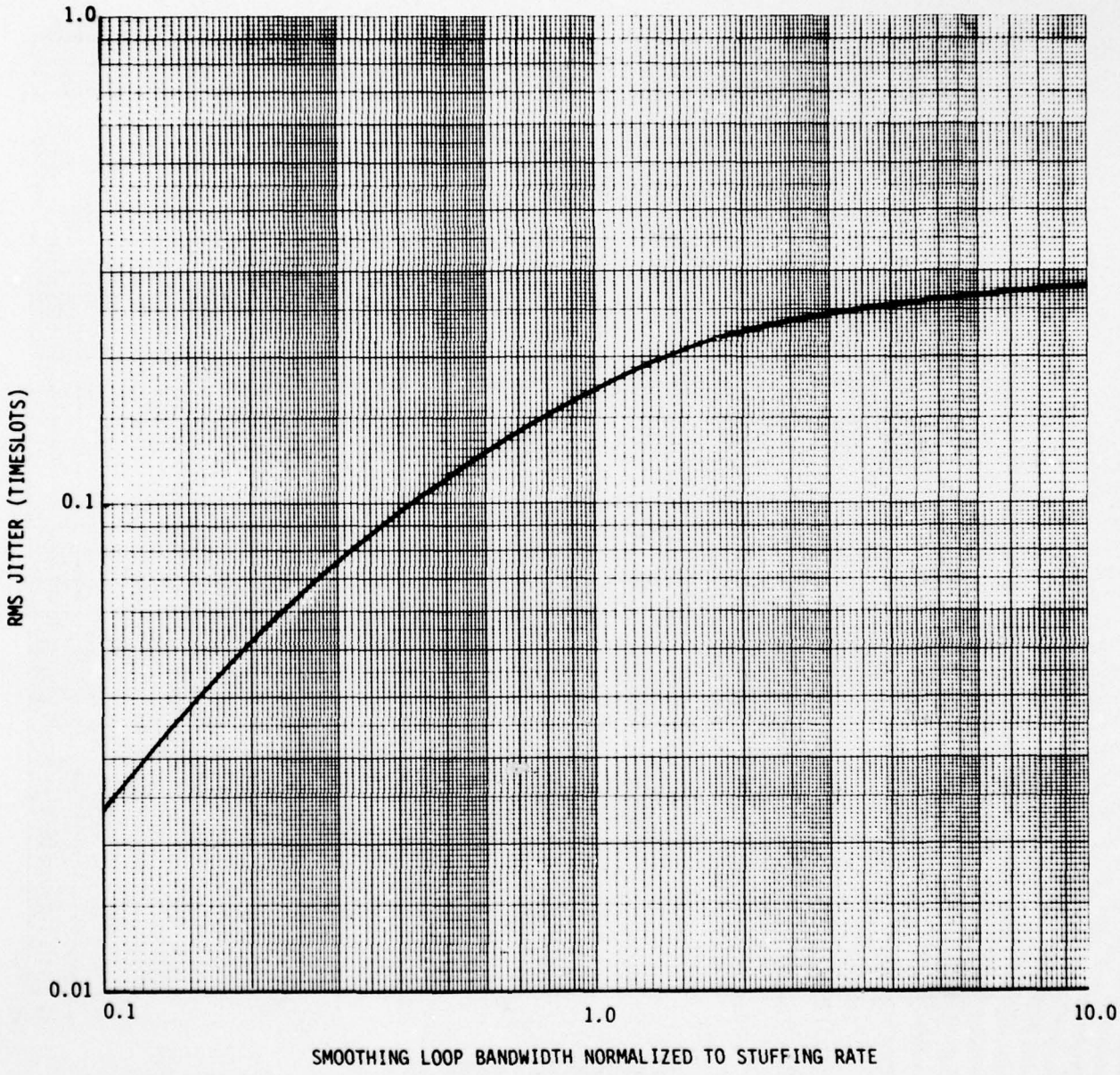


Figure 5.1.2-2. RMS Jitter at First Order Smoothing Loop Output

AD-A049 310 HARRIS CORP MELBOURNE FLA ELECTRONIC SYSTEMS DIV F/G 17/2
ANALYSIS OF JITTER CHARACTERISTICS IN A PULSE STUFFING TDM NETW--ETC(U)
JUN 77 J A GRACIA, T G ZOGAKIS DCA100-76-C-0072
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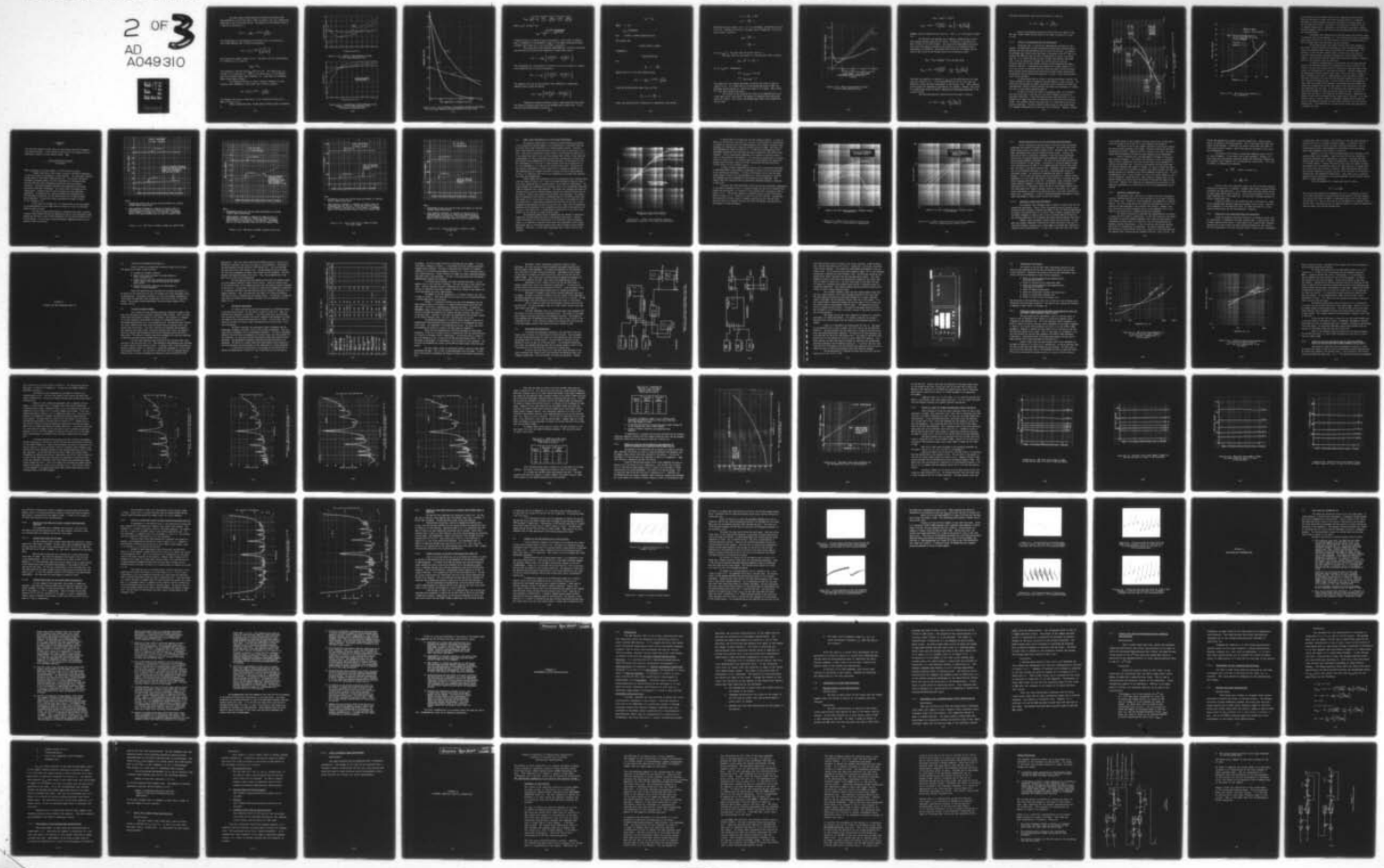


The actual phase jittered waveform attributed to stuffing jitter when smoothed by a first order loop is shown in Figure 5.1.2-3 for a time period normalized to the stuffing rate period. The equation for the stuffing jitter as a function of time and f_c is

$$y(t) = t - \frac{1}{2\pi f_c} + e^{-2\pi f_c t} \frac{e^{-\pi f_c}}{1-e^{-2\pi f_c}} \quad .$$

The instantaneous bit rate waveforms for stuffing jitter at the output of a first order smoothing loop is given by the equation

$$f(t) = 1-2\pi f_c \; e^{-2\pi f_c t} \left(\frac{e^{-\pi f_c}}{1-e^{-2\pi f_c}} \right) .$$

These results are shown in Figure 5.1.2-4. The peak-to-peak bit rate deviation as a function of f_c is given by

$$\Delta f_{max} = 2\pi f_c \quad .$$

This expression is derived from $\Delta f_{max}=f(0.5)-f(-0.5)$. This implies that Δf is a factor of 2π larger than f_c. Figure 5.1.2-4 shows that Δf is not centered about the tributary channel input frequency, f=0. (Note these are incremental models around nominal values.)

The frequency slew rate, or rate of change of frequency, for the stuffing jitter smoothed by a first order loop is given by equation

$$s(t) = (2\pi f_c)^2 \; e^{-2\pi f_c t} \quad \frac{e^{-\pi f_c}}{1-e^{-2\pi f_c}} \quad .$$

The frequency slew rate as a function of f_c for a stuffing rate time slot is shown in Figure 5.1.2-5.

Using a second-order loop, the RMS output stuffing jitter is expressed as

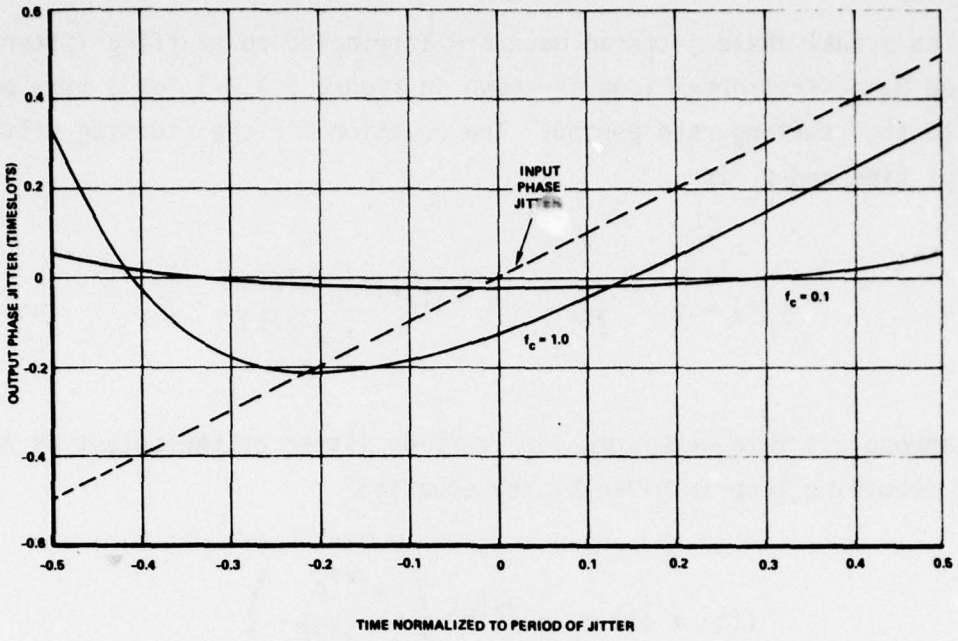


Figure 5.1.2-3. Stuffing Jitter Waveform at Output of First Order Smoothing Filter

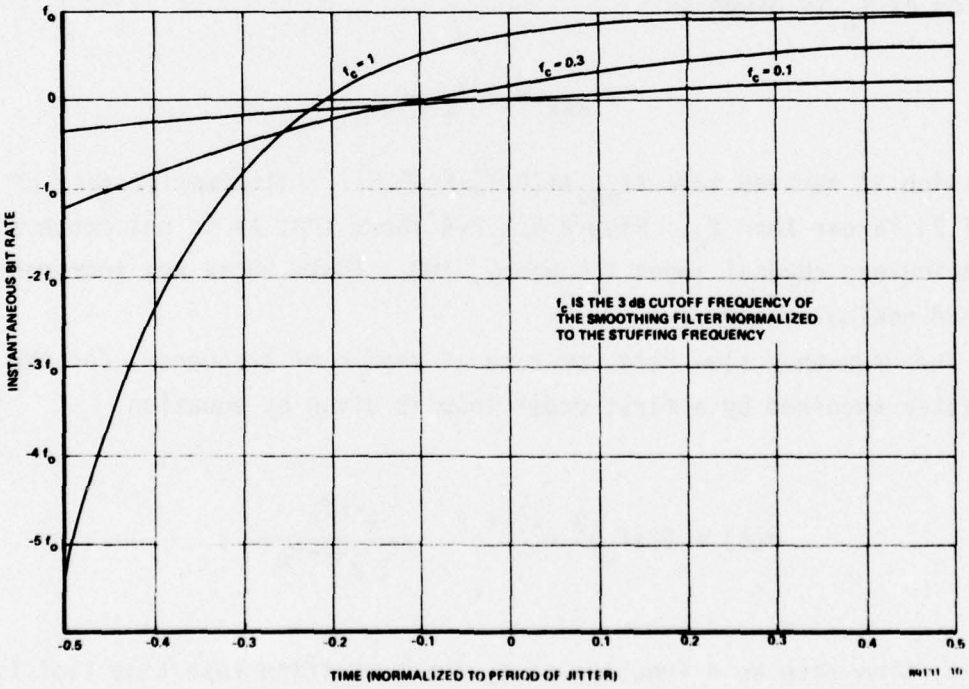


Figure 5.1.2-4. Instantaneous Bit Rate Waveform at the Output of a First Order Smoothing Filter Attributed to Stuffing Jitter

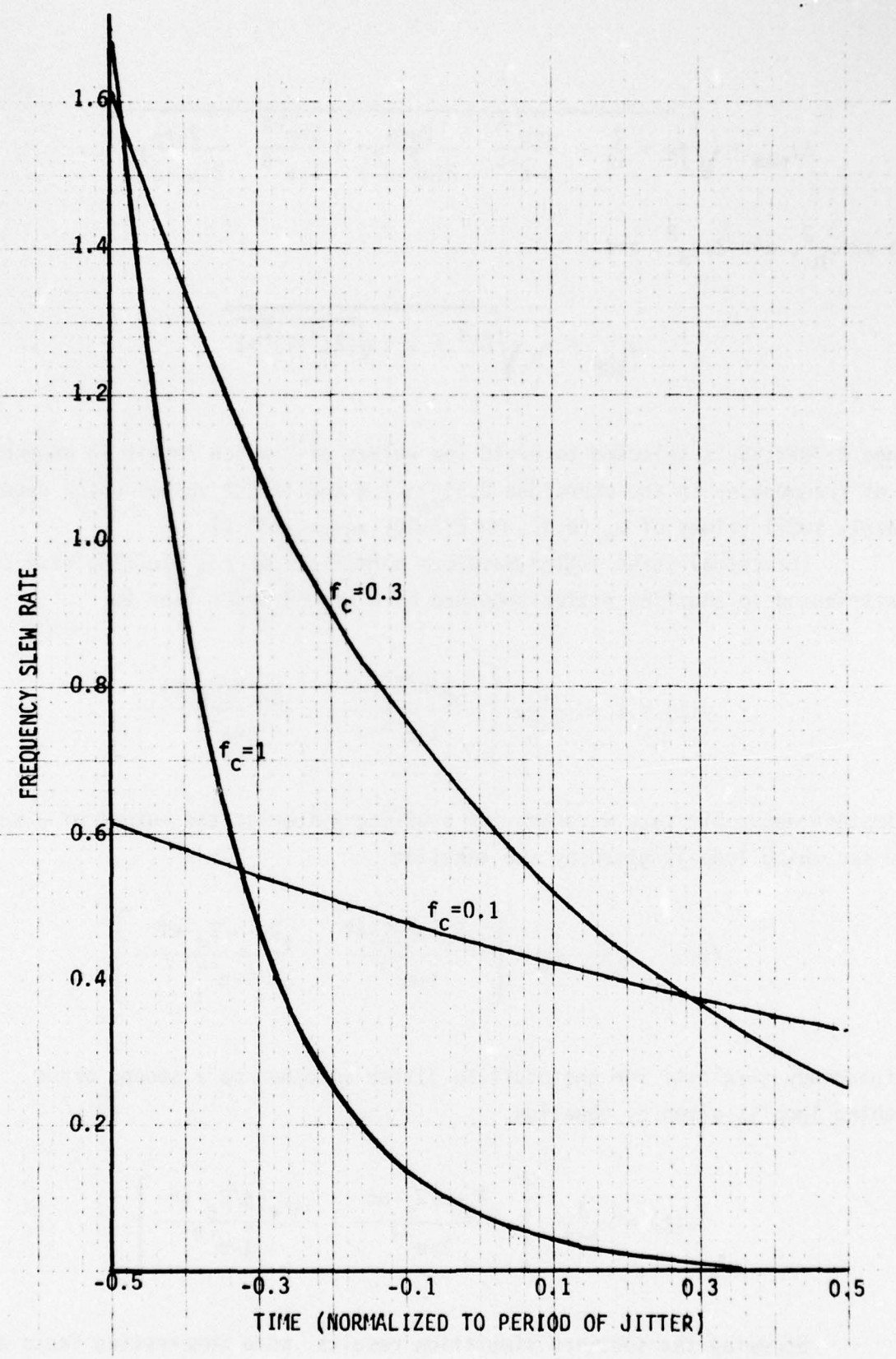


Figure 5.1.2-5. Rate of Change of Instantaneous Bit Rate at the Output of a First Order Smoothing Loop Attributed to Stuffing Jitter

$$\Delta y_{rms} = \sqrt{\frac{1}{12} + \frac{2}{\alpha\beta} - \frac{1+e^{-\alpha}}{1-e^{-\alpha}} \quad \frac{2\beta+\alpha}{2(\alpha^2-\beta^2)} + \frac{1+e^{-\beta}}{1-e^{-\beta}} \quad \frac{2\alpha+\beta}{2(\alpha^2-\beta^2)}} \quad ,$$

where $\alpha\beta=\omega_n^2$, $\alpha+\beta=2\omega\zeta_n^2$, and

$$\omega_{3dB} = \omega_n \sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2+1)^2+1}} \quad .$$

A range $0.707 \leq \zeta \leq 5$ is selected to avoid low values of ζ which result in enhancement of frequencies in the bandwidth $0.5 \leq \frac{\omega}{\omega_n} \leq 1.4$ and larger values which require extremely small values of ω_n (e.g., for $\zeta=5.00$, $\omega_n=\omega_{3dB}/10.1$).

The actual phase jitter waveform normalized over a stuffing rate period and attributed to stuffing jitter smoothed by a second order loop is

$$y(t) = t + \frac{1}{\alpha-\beta}\left[\frac{\alpha e^{-\alpha/2} e^{-\alpha t}}{1-e^{-\alpha}} - \frac{\beta e^{-\beta/2} e^{-\beta t}}{1-e^{-\beta}}\right].$$

The instantaneous bit rate waveform for stuffing jitter at the output of a second order smoothing loop is given by the equation

$$f(t) = 1 + \frac{1}{\alpha-\beta}\left[\frac{\beta^2 e^{-\beta/2} e^{-\beta t}}{1-e^{-\beta}} - \frac{\alpha^2 e^{-\alpha/2} e^{-\alpha t}}{1-e^{-\alpha}}\right].$$

The frequency slew rate for the stuffing jitter smoothed by a second order smoothing loop is given by equation

$$s(t) = \frac{1}{\alpha-\beta}\left[\frac{\alpha^3 e^{-\alpha/2} e^{-\alpha t}}{1-e^{-\alpha}} - \frac{\beta^3 e^{-\beta/2} e^{-\beta t}}{1-e^{-\beta}}\right].$$

Studying the software simulation results, some interesting facts about the effects of waiting time jitter on the smoothed output jitter arise. First, note that the stuffing period is given by

$$T_{SP} = n\, T_{SO} .$$

Where, $n = \frac{1}{\rho}$,

$T_{SO} = 1/(\text{SO RATE})$,

and SO RATE = Stuffing opportunity rate.

Next observe that

$$m<n<m+1, \text{ where } n \neq \text{integer} .$$

Consequently,

$$mT_{SO}<nT_{SO}<(m+1)T_{SO} ,$$

and

$$\frac{m}{n} < 1 < \frac{m+1}{n} .$$

Observe that for a first order smoothing loop

$$y(t) = t - \frac{1}{2\pi f_c} + e^{-2\pi f_c t} \frac{e^{-\pi f_c}}{1-e^{-2\pi f_c}} .$$

Using the stuffing period range $-\frac{1}{2}<t<\frac{1}{2}$, we find

$$\frac{m}{n} - \frac{1}{2} < \frac{1}{2} < \frac{m+1}{n} - \frac{1}{2} .$$

Hence, the stuffing period is modified to a combination of two periods

$$-\tfrac{1}{2} < t < \frac{m}{n} - \tfrac{1}{2} \quad \text{and}$$

$$-\tfrac{1}{2} < t < \frac{m+1}{n} - \tfrac{1}{2} \ .$$

Observing that $0 \leq \rho \leq 1$; hence, $1 < n < \infty$. If n is a noninteger, the smallest value of n is $n = 1+\varepsilon$. Setting m=1 and m+1=2, the upper limit of normalized t in y(t) for the m+1 stuff is given by

$$t_{max} = \frac{m+1}{n} - \tfrac{1}{2}$$

$$= \frac{2}{1+\varepsilon} - \tfrac{1}{2} \ .$$

As $\varepsilon \to 0$, $t_{max} \to 1.5$. The lower limit for the m+1 stuff is 1.

The upper limit for the m stuff is 1, and the lower limit is given by

$$t_{min} = \frac{m}{n} - \tfrac{1}{2} = \frac{1}{1+\delta} - \tfrac{1}{2} \ .$$

As $\delta \to 1$, $t_{min} \to 0.0$. Consequently,

$$0.0 < t_{\text{m stuff}} < 0.5, \text{ and}$$

$$0.5 < t_{\text{m+1 stuff}} < 1.5 \ .$$

The equation for y(t) showing the effect of waiting time jitter is given in Figure 5.1.2-6. It is noted that as $\rho \to 0$ the maximum deviations of $\frac{m+1}{n}$ and $\frac{m}{n}$ becomes smaller because $n \to \infty$ and the two ratios $\to 1$ as a bound. Small values of ρ have lower waiting time jitter.

For $m < n < m+\frac{1}{2}$, as was noted earlier, there is an immediate build up of jitter when the m+1 stuff occurs. The sequence is gradually reset during the series of m stuffs. For $m < n < m+1$, the maximum phase jitter can be computed for the m+1 stuff

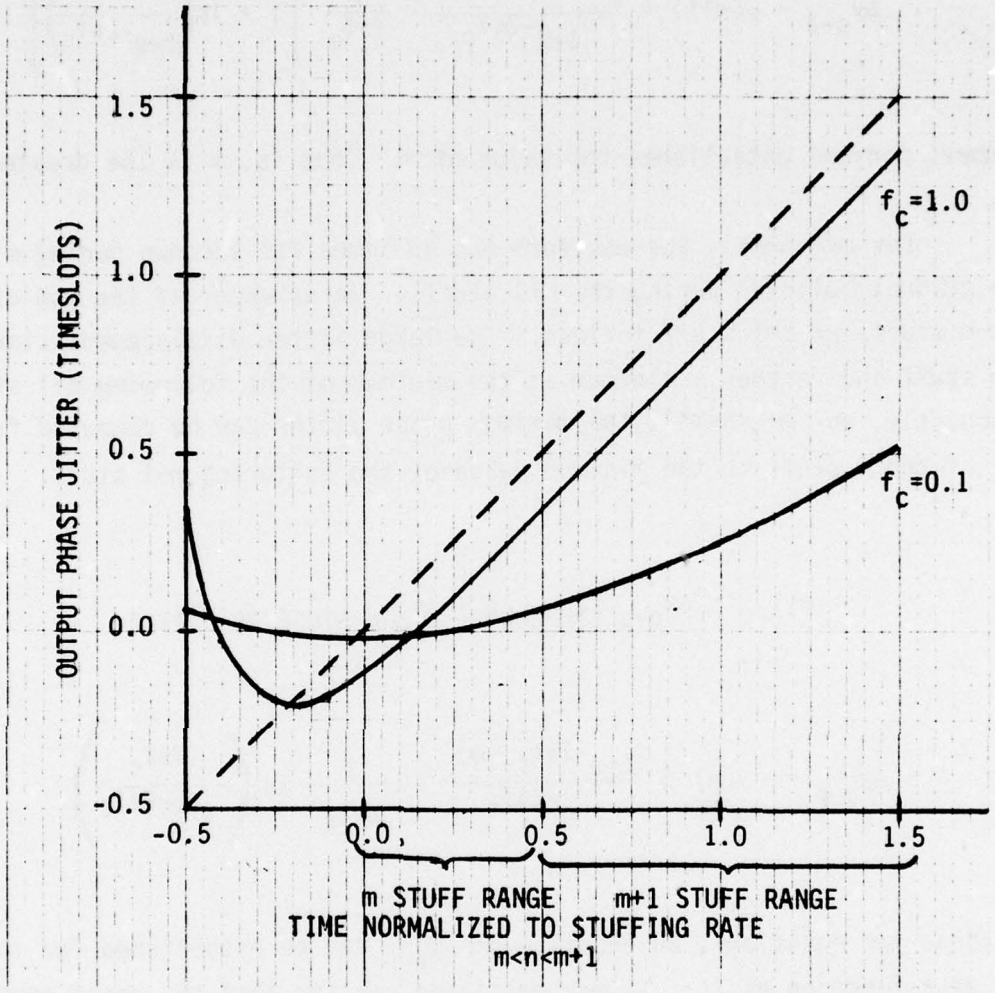


Figure 5.1.2-6. Phase Jitter Waveform at Output of First Order Smoothing Filter

$$\Delta y_{p-p} = y_{max}(t) - y_{min}(t) .$$

$$\Delta y_{p-p} = \rho(m+1) + \frac{e^{-2\pi f_c \rho(m+1)}}{1-e^{-2\pi f_c}} - \frac{1}{2\pi f_c} \left[1 + \ln\left(\frac{2\pi f_c}{1-e^{-2\pi f_c}}\right)\right] .$$

Remember, $m<n<m+1$ establishes the value of m. That is, m is the greatest integer in n.

For $m+\frac{1}{2}<n<m+1$, the waveform has an immediate letdown during m stuffs and a gradual build-up during the m+1 stuffs. In essence, at the end of the short m stuff, an m+1 stuff follows. The large jitter displacement starts with the m stuff and reaches a minimum at the minimum of the following m+1 stuff. Consequently, for $m+\frac{1}{2}<n<m+1$, the maximum phase jitter can be computed from the start of the m stuff to the minimum value of the following m+1 stuff.

$$\Delta y_{p-p} = \Delta y_{p-p \text{ STEPDOWN}} + \Delta y_{p-p \text{ STUFFING JITTER}}$$

$$\Delta y_{p-p} = -\rho(m) + \frac{2-e^{-2\pi f_c \rho(m)}}{1-e^{-2\pi f_c}} - \frac{1}{2\pi f_c} \ln\left(\frac{2\pi f_c}{1-e^{-2\pi f_c}}\right) .$$

From these two equations, an equation of Δy_{p-p} can be established for the range $0 \leq \rho \leq 1$ as a function of f_c. It was mentioned earlier that the reset does not necessarily return the phase displacement to the original value. These equations do not account for subharmonics generated by this sequence. However, this jitter is a second order effect and doesn't generate the displacement magnitudes of the m and m+1 stuffs.

The time associated with rapid build-up for $m<n<m+\frac{1}{2}$ is given by

$$\Delta t = \rho(m+1) - \frac{1}{2\pi f_c} \ln\left(\frac{2\pi f_c}{1-e^{-2\pi f_c}}\right) .$$

The time associated with rapid reset for $m+\frac{1}{2}<n<m+1$ is given by

$$\Delta t = \rho(m) + \frac{1}{2\pi f_c} \ln \frac{2\pi f_c}{1-e^{-2\pi f_c}} .$$

Results of experiments varying the cutoff filter for models of the Bell M12, VICOM T1-4000, and the AN-GSC-24 are shown in Figure 5.1.2-7 and 5.1.2-8.

5.1.3 Effects of Cascading Second Level Multiplexers

Duttweiler (Ref. 2) had the most comprehensive discussion on this subject. He established an upper bound based on theoretical spectrum analysis approach and then used experimental data to verify his analysis. In essence, he concluded that the RMS jitter amplitude at the output of the N^{th} node is no greater than $\sqrt{N/6}$, and that the rate of accumulation of jitter is no faster than $\sqrt{N}$. It is further pointed out that to obtain this bound on the growth rate, it was not necessary to assume the stuffing ratios at each synchronizer identical nor the transfer function of each desynchronizer (demultiplexer) identical. Experimental data gathered for cascade lengths of 1, 2, 4, 8, and 16 over six different stuffing ratios were used to prove the bound. While no data inconsistencies were noted with the upper bound, some data was inconsistent with the predicted accumulation of jitter. These inconsistencies could not be explained.

In pursuing the study of jitter in cascaded multiplexer networks, the effort resorted to a GASP IV computer simulation, MUXJIT, to derive results. The difficulty with handling the effort analytically arises from the fact that the required model involves variable discrete time events and continuous bit streams. This task is more readily handled by MUXJIT.

In order to isolate the effect of cascading jitter, it is necessary that the effects due to stuffing ratio and offset frequency variations be absolutely controlled. It was discussed previously that variations in offset frequency will impact the effect of smoothing loop filtering on the stuffing jitter. The tributary channel input data rate is a single source and was considered isochronous. The data transport digital rates for the various nodes of a hardware implementation are more than likely different. However, allowing

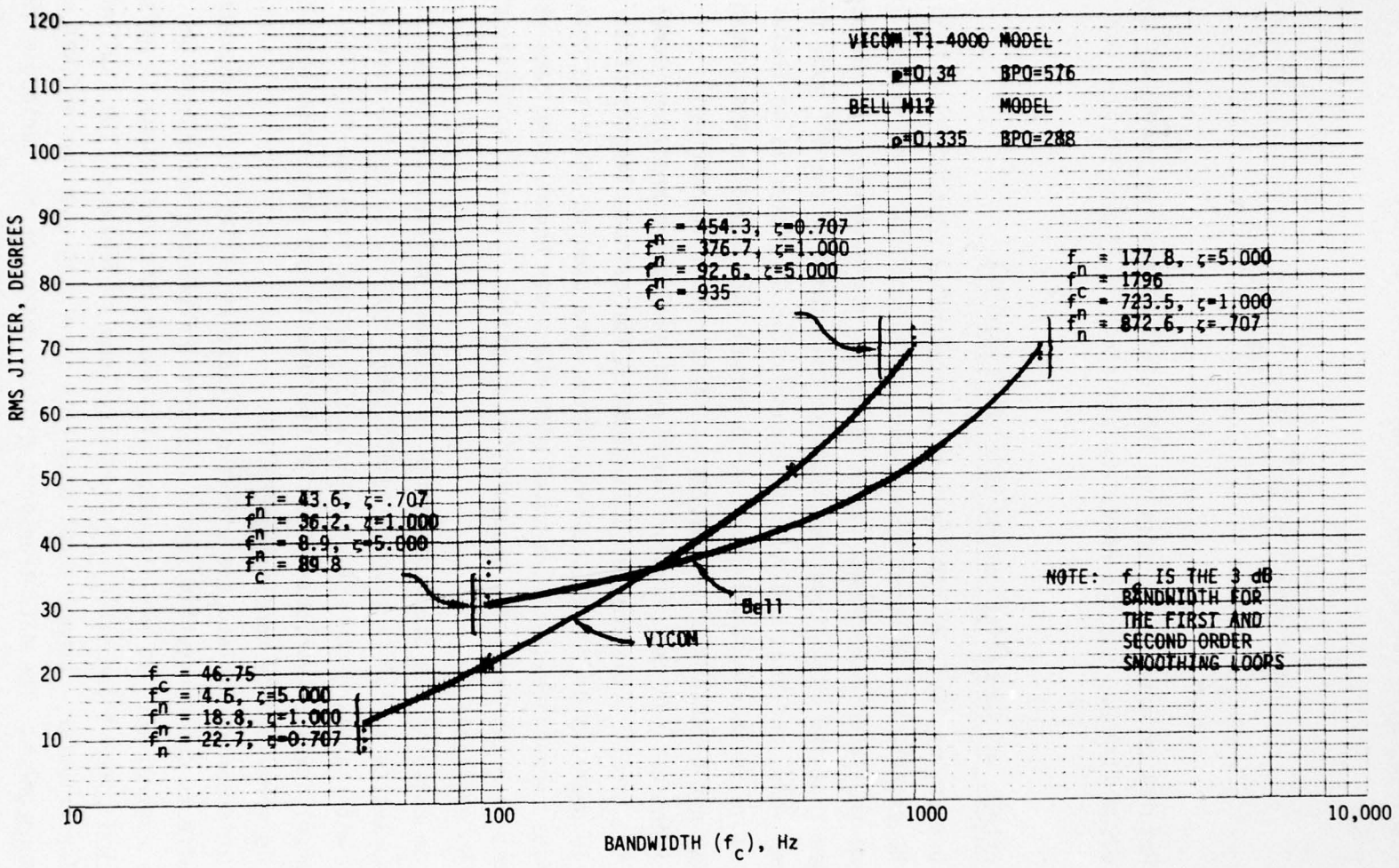


Figure 5.1.2-7. RMS Jitter Versus Bandwidth (f_c) for the Bell M12 and VICOM T1-4000

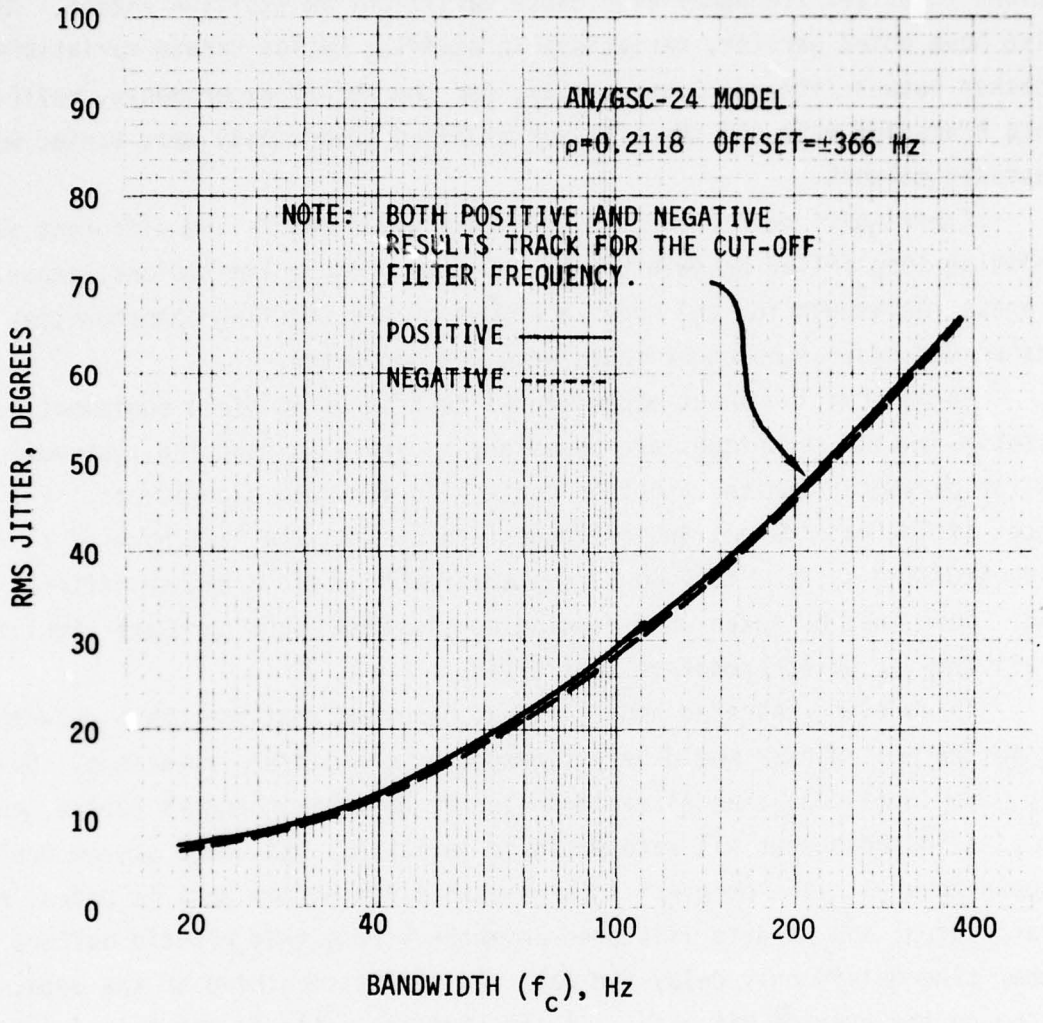


Figure 5.1.2-8. RMS Jitter Versus Bandwidth (f_c) for the AN/GSC-24

such variations in the software simulator will compound the data reduction and limit the ability to draw conclusions from such efforts. In addition, variations in offset frequency also cause variations in stuffing ratios. As has also been noted earlier, variations in stuffing ratios create variations in smoothed output jitter. Consequently, for the MUXJIT experiments, neither the data transport rate nor the bits per stuffing opportunity were varied within the cascaded network.

Experiments were conducted using different models and different values of smoothing loop filter bandwidths, f_c. Due to program limitations, experiments using phase variations for the node locations of the stuffing opportunities as well as second order loop experiments were not conducted.

An observation about experimental testing using field equipment is that static testing techniques are necessary to avoid introducing systematic errors for parameters which cannot be controlled for such experiments. For instance, if low rate data transport nodes are used as the last node of a positive stuffing system, they would systematically yield a higher jitter reading. Care must be taken when drawing conclusions about hardware simulators where all the variables cannot be controlled.

In modeling cascaded nodes, it was observed that the phase detector output in the multiplexer would be influenced by the jitter variations. Obviously, the input data channel would no longer be an isochronous source, but, rather, its instantaneous bit rate would be variable. This data stream would be mesochronous with the original input signal since no new data is added, no data is deleted, and no data is stored anywhere. Note that elastic buffers and other time delays only delay the data and permit smoothing of the data, but don't change the average bit rate. If the stuffing ratio is maintained constant, then the average offset frequency (the average difference between the stable data transport rate and the input channel rate) and the bits per stuffing opportunity are the same. If the average offset frequency remains the same, then the number of stuffs per period remains the same. The only difference that can occur is the length of the stuffing periods. Meanwhile, the number of stuffs and the average stuffing length remains the same. It has been observed that for a given ρ with an isochronous tributary input channel and $m<n<m+1$, the waveform consisted of stuffs which occurred at m or m+1 stuffing opportunities. The combination of m stuffs and m+1 stuffs were controlled by a sequence such that

$$n = \frac{\alpha m+\beta(m+1)}{\alpha+\beta} \quad .$$

$\alpha+\beta$, the total number of stuffs, which is controlled by the offset frequency, also remains constant. It was speculated that possibly the sequence could be modified to include m-1 stuffs and m+2 stuffs. Then,

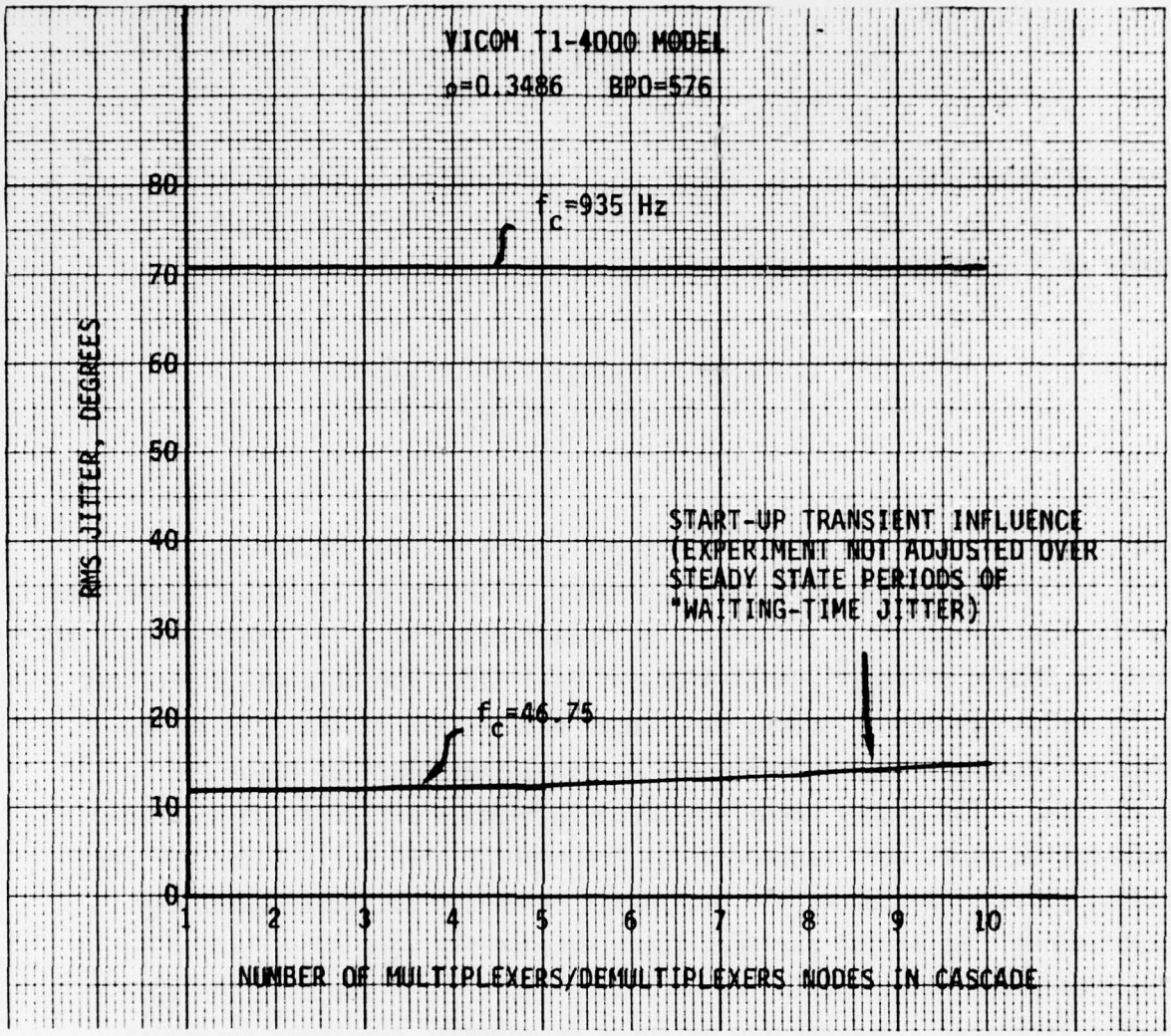
$$n = \frac{a_1(m-1)+a_2(m)+a_3(m+1)+a_4(m+2)}{a_1+a_2+a_3+a_4} \quad ,$$

where $a_1+a_2+a_3+a_4$ is the total number of stuffs during the period.

A major revelation of this study, elicited by the MUXJIT experiments, is that jitter does not accumulate in tandem networks. The experiments conducted include models of the VICOM T1-4000 and Bell M12. The original experiments indicated a cascading impact, but closer examination of the results show that the statistics were influenced by simulation start up transient variations. The higher bandwidth smoothing loop experiments using proper observation times were reconducted. The results show no influence of cascading jitter. Resources did not permit rerunning the lower bandwidth experiments. As stated earlier, these experiments were conducted using the same phase relationship for each node location of the stuffing opportunity parameter. The results of these experiments are shown in Figure 5.1.3-1 through 5.1.3-4.

Actual tests run by RADC (Ref. 16) revealed that jitter measurements for cascaded networks do not always show an increase in jitter for increased number of nodes in tandem.

The task of analyzing the effects of cascading jitter with a variable tributary input channel rate was not addressed as part of this preliminary study. Neither was the case of small offset frequencies for the positive-negative class of multiplexers. In such cases, perhaps additional compensating positive and negative stuffs could result.



NOTES:

1. EXPERIMENTAL RESULTS ONLY FOR ONE PHASE RELATIONSHIP OF STUFFING INTERVAL AMONG CASCADE NODES.

2. LOWER FREQUENCY EXPERIMENT IS IMPACTED BY START-UP SINCE ITS EXPERIMENTS WERE NOT PRECISELY STARTED AND TERMINATED OVER A PRECISE NUMBER OF "WAITING TIME" JITTER PERIODS. FURTHERMORE PARTS OF THE PERIOD APPEARED FROM THE START-UP TRANSIENT AREA.

Figure 5.1.3-1. RMS Jitter vs Number of Nodes for VICOM T1-4000

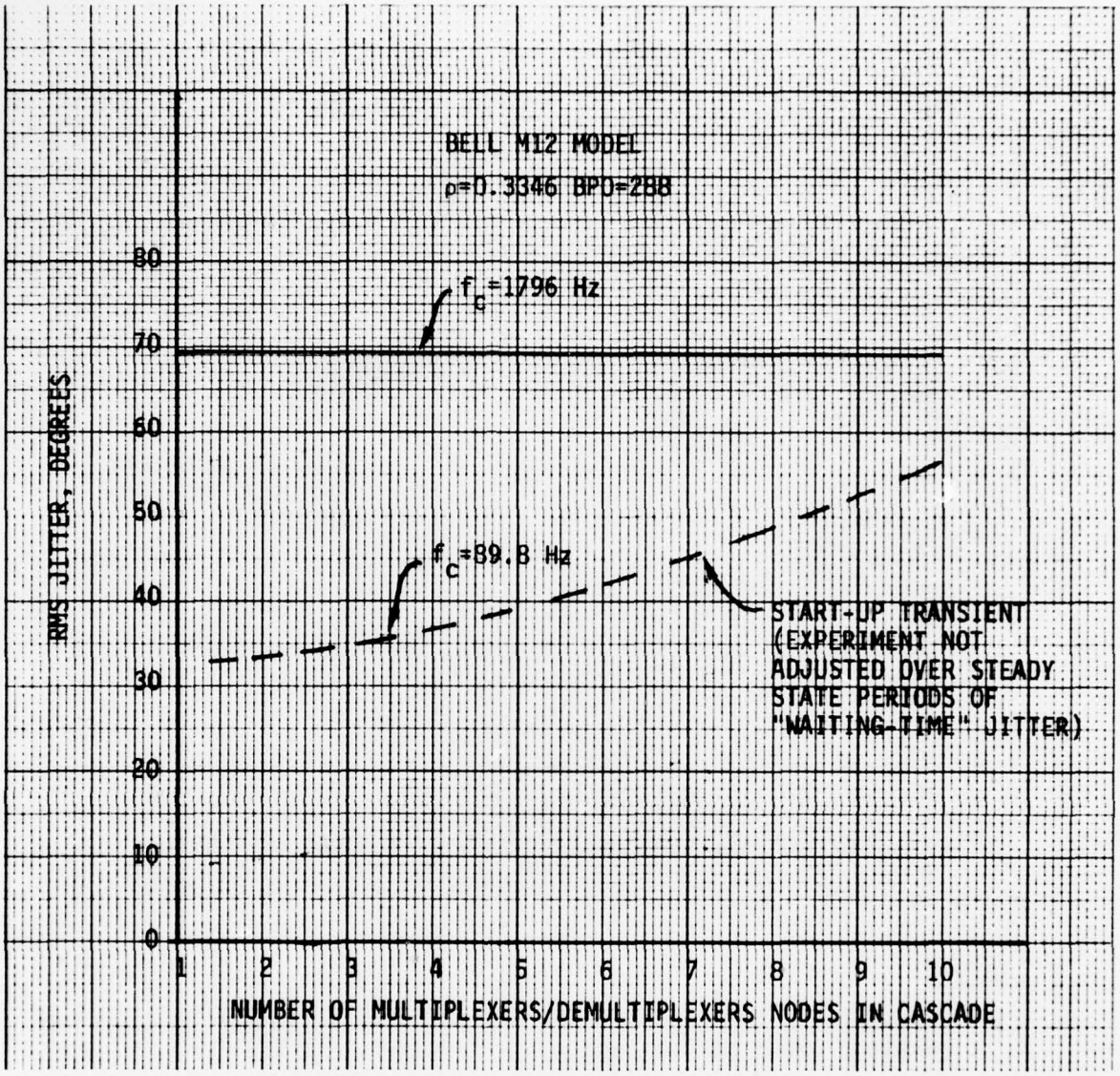


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Figure 5.1.3-2. RMS Jitter vs Number of Nodes for Bell M12

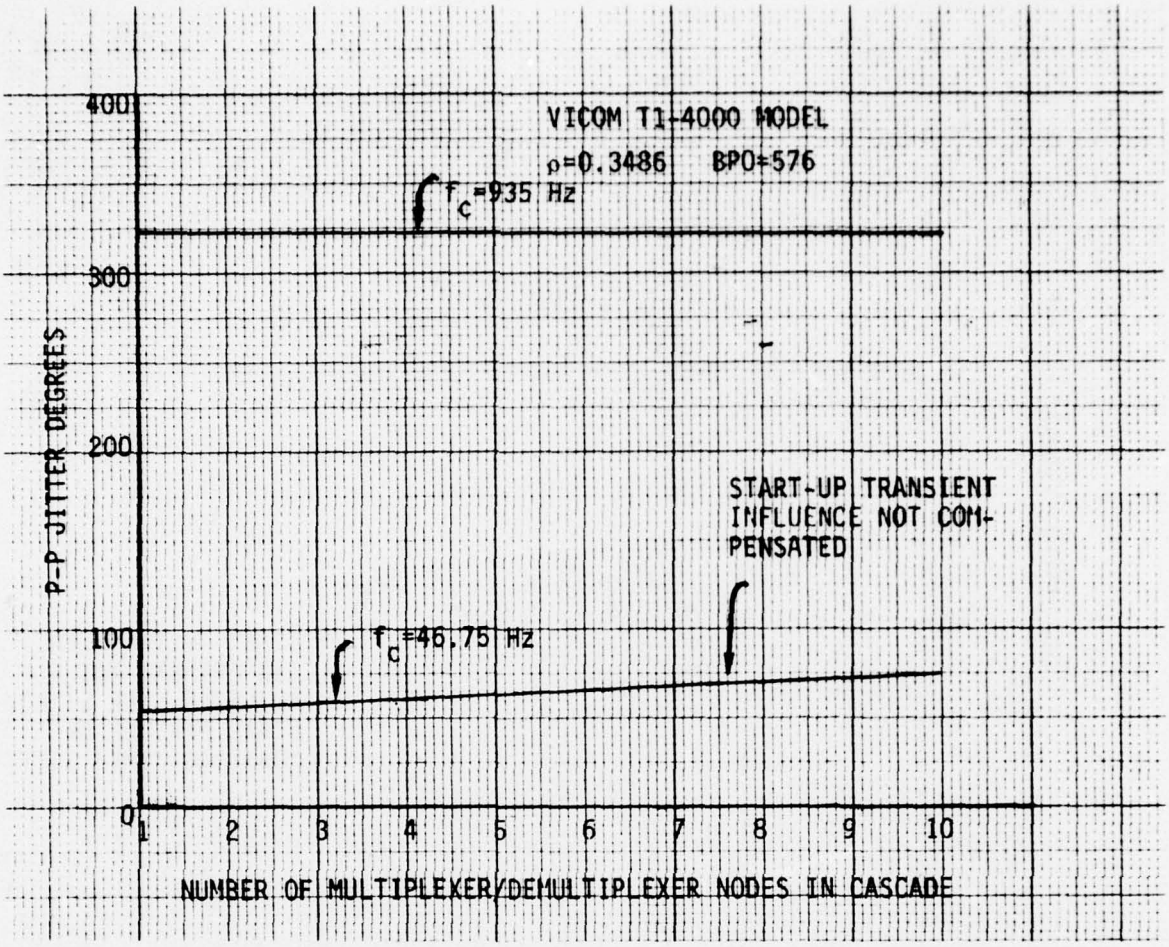

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Figure 5.1.3-3. Peak to Peak Jitter vs Number of Nodes for VICOM T1-4000

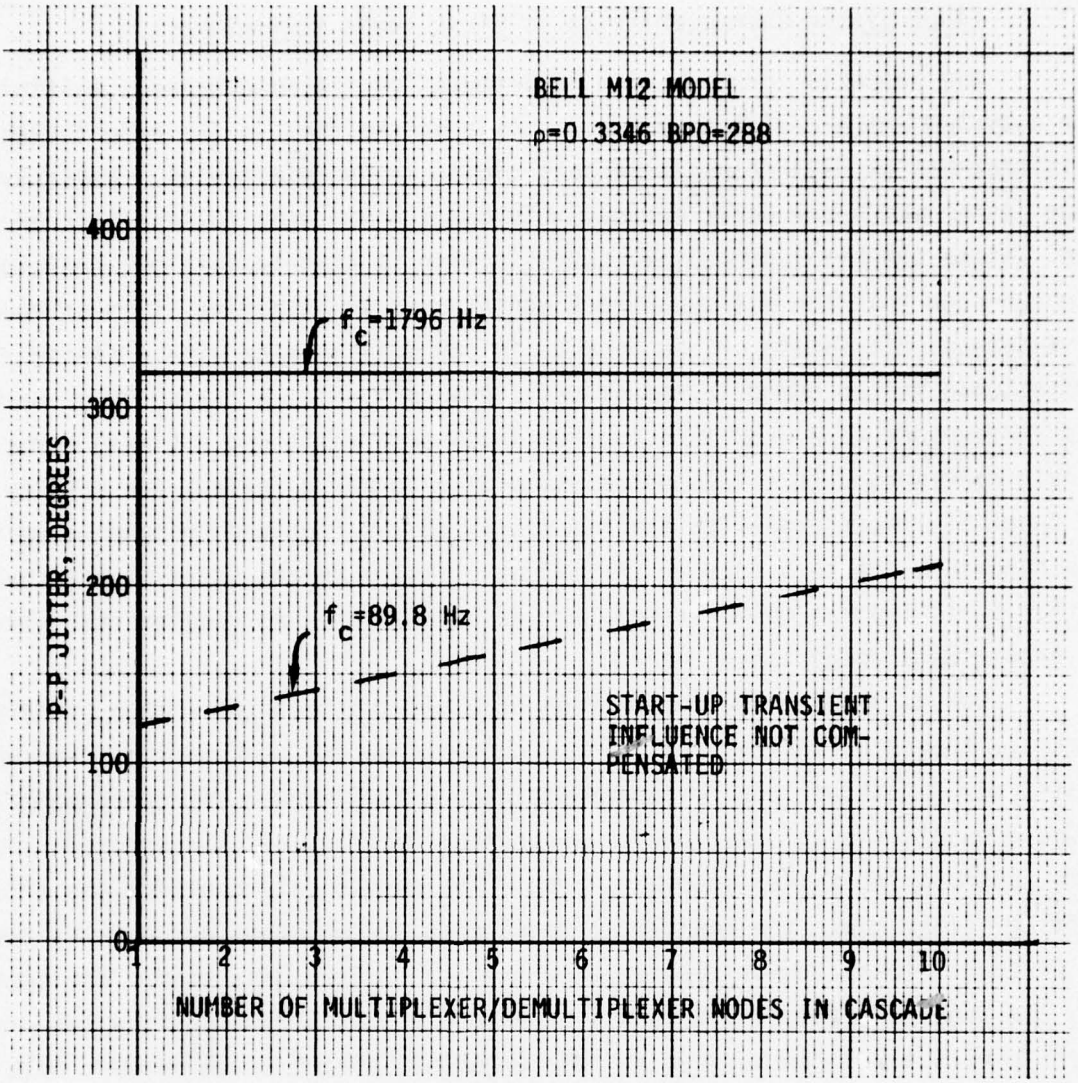

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Figure 5.1.3-4. Peak to Peak Jitter vs Number of Nodes for Bell M12

5.2 Input Jitter Characteristics of First Level Multiplexers

One potential problem area in integrating the mesochronous multiplexer into a system which contains modems or bit synchronizers is the effect that the bit jitter has on data transmission bit timing recovery circuits. Excessive input jitter which may occur can possibly cause a bit sync to lose lock or slip bits. Since the bit synchronizer output timing is used to make bit decisions, it is not enough that the bit sync track the average input timing, it must track the instantaneous bit timing or the data decisions will be made with a timing error. With matched filter demodulation of unfiltered NRZ data, a timing error of 0.25 bits corresponds to a 6 dB loss in signal-to-noise ratio and a timing error of 0.1 bit corresponds to a 1.9 dB loss in signal-to-noise ratio. The ability of the input bit synchronizer to track input jitter is improved by opening up its loop bandwidth but this impacts the effect of noise on the bit timing recovery so that it is imperative that the bit sync bandwidth be no greater than necessary for proper data demodulation.

Curves showing the interaction of a bit synchronizer with a jittered input clock are shown in Figure 5.2-1. These curves show the peak timing error when a first order smoothing loop is interfaced with a first order bit synchronizer. The figure presents the information for a constant ratio of bit synchronizer loop bandwidth to smoothing filter loop bandwidth. The curves only consider the effects of stuffing jitter since the analytical model used did not consider waiting time jitter effects. These curves clearly show the effect just discussed. For example, when the smoothing filter loop has a bandwidth equal to the stuffing rate, which from Figure 5.1.2-1 can be seen to have an output jitter of 55 percent of a bit, the timing error is significantly decreased only when the bit sync has a large bandwidth of approximately 10 times the stuffing rate. When the bit synchronizer bandwidth and the smoothing filter bandwidth are both equal to the stuffing rate ($k=1, f_c=1$), the timing error is approximately 30 percent of a bit, which corresponds to an 8.0 dB loss in signal-to-noise ratio.

The preceding example serves to demonstrate the concept of interaction between the jittered output and the bit synchronizer timing error. However, since the principal of a bit synchronizer is to faithfully track the incoming signal, it is desired to avoid the static phase error generated in first order phaselocked loops by differences between input signal frequency and VCO nominal frequency. Therefore, a second order phaselocked loop is used in the bit synchronizer.

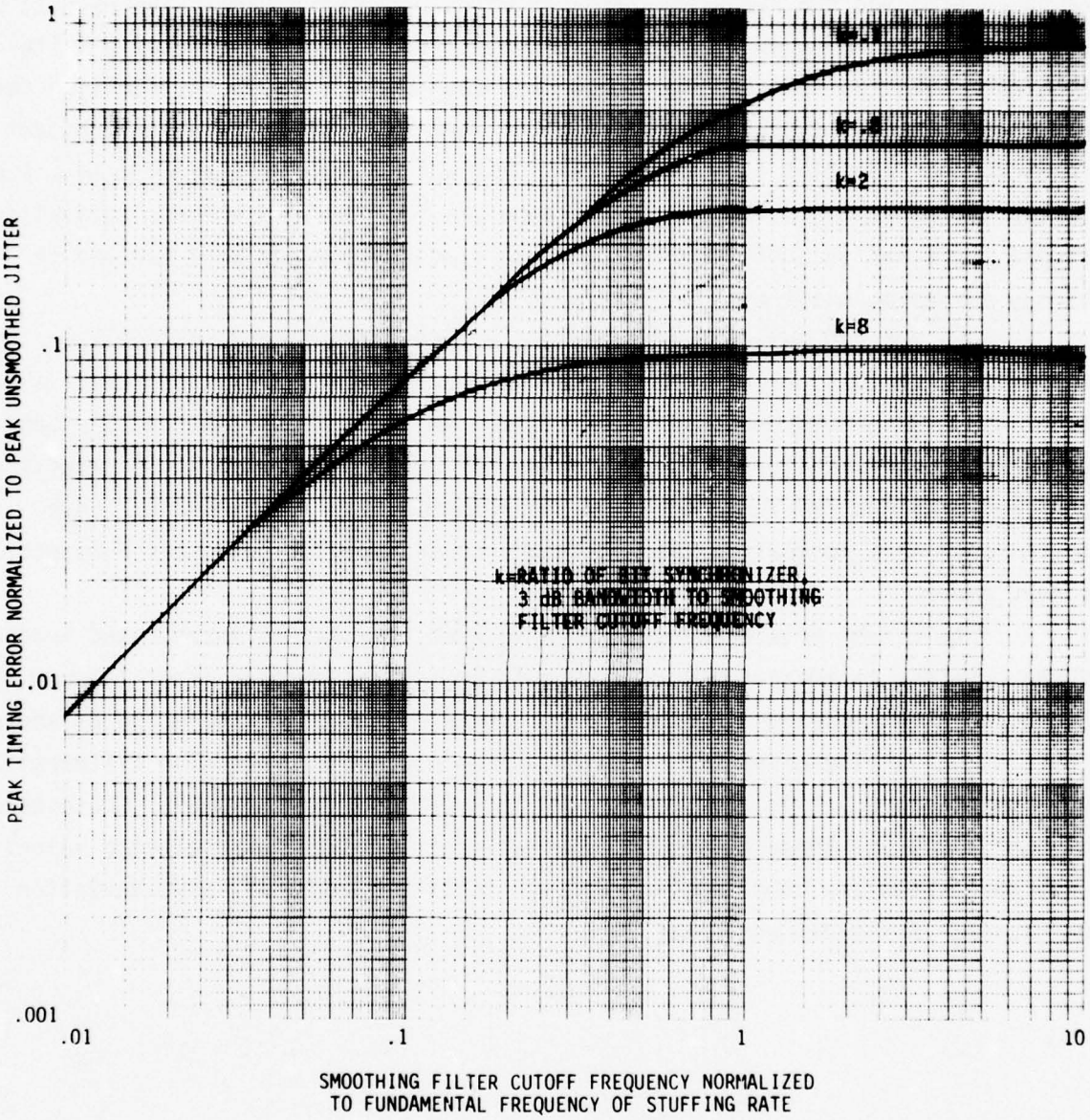


Figure 5.2-1. Effect of Pulse Stuffing Jitter on Data Recovery Timing for a First Order Bit Synchronizer

A second order bit synchronizer has been modeled on MUXJIT. In order to obtain an illustration of the impact of jitter on a second order bit synchronizer an example was selected using the VICOM parameters with a nominal tributary input frequency of 1.544 MHz and a resulting stuffing ratio of 0.3486. The results of this experiment are shown in Figure 5.2-2. In the figure the smoothing filter bandwidths selected for the experiment have been normalized to the stuffing rate frequency. The bit synchronizer bandwidths were selected to maintain constant ratios to the smoothing loop bandwidth. This was done to present data in a format similar to Figure 5.2-1. The results shown are for peak phase error (deviation) between input and output signals of the bit synchronizer and were derived by fitting curves to a set of MUXJIT outputs.

In order to better understand the effects of bit synchronizer bandwidths, an additional MUXJIT output format is presented in Figure 5.2-3 for fixed values of bit synchronizer bandwidths. It differs from Figure 5.2-2 in that the bandwidths shown in Figure 5.2-3 are presented for a fixed relationship of stuffing rate frequency and are independent of the smoothing filter bandwidth. Both figures show that increasing the bit synchronizer bandwidth produces a reduction in peak error.

The curves have been normalized so that they can be interpreted independently of the specific parameters used. It should be noted that peak error induced by the second level multiplexer is a function of the stuffing ratio, selected as shown in Figure 5.1.1-1. The effects induced by a smoothing filter are also different as shown in Figure 5.1.2-7. Figures 5.2-2 and 5.2-3 are for ρ=0.3486. Consequently, the application of these curves is somewhat restricted by this selected value. Since the curves are compiled from data collected from MUXJIT, some deviation is anticipated in fielded equipment.

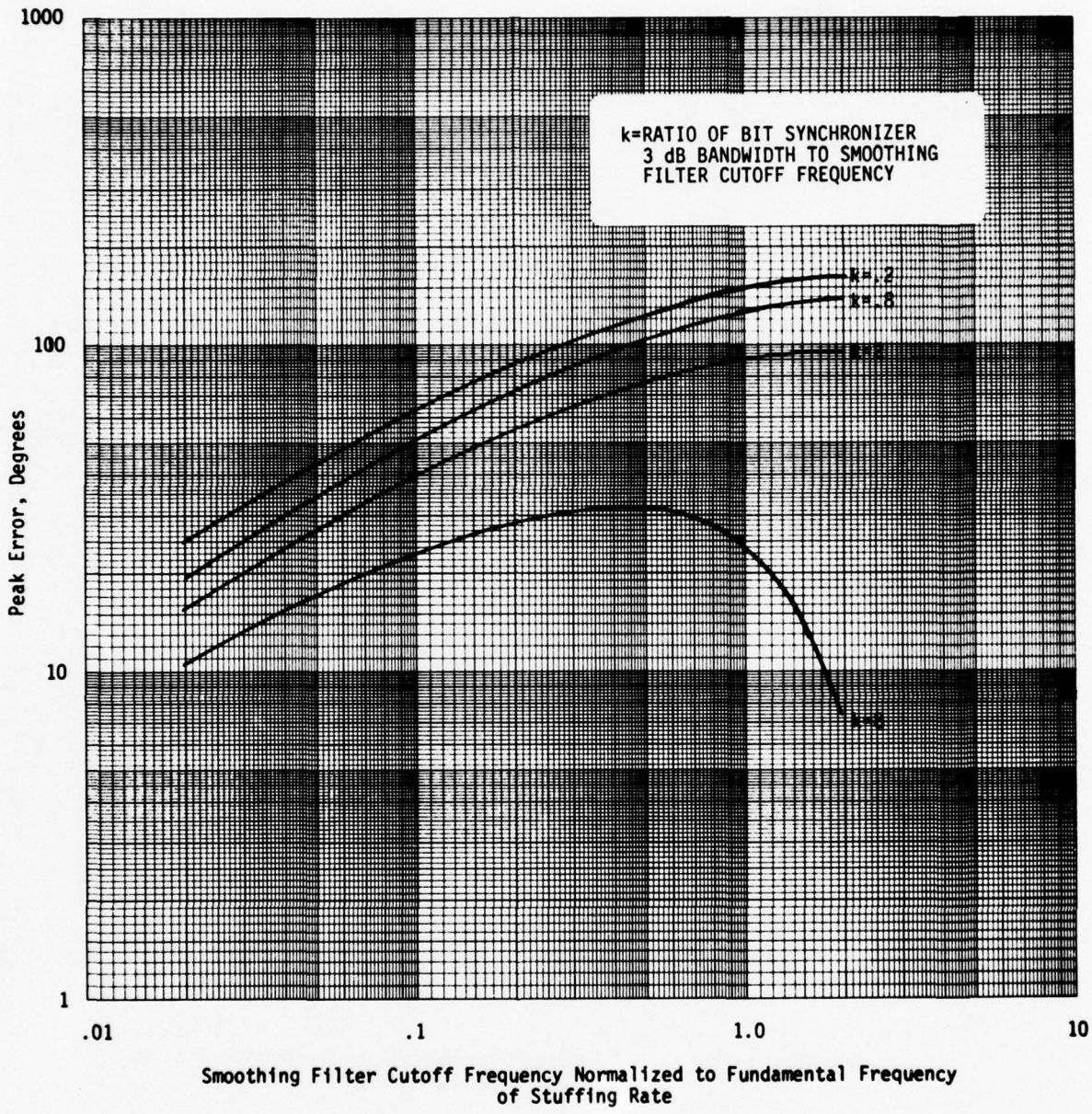


Figure 5.2-2. Effect of Pulse Stuffing Jitter on Data Recovery Timing for a Second Order Bit Synchronizer

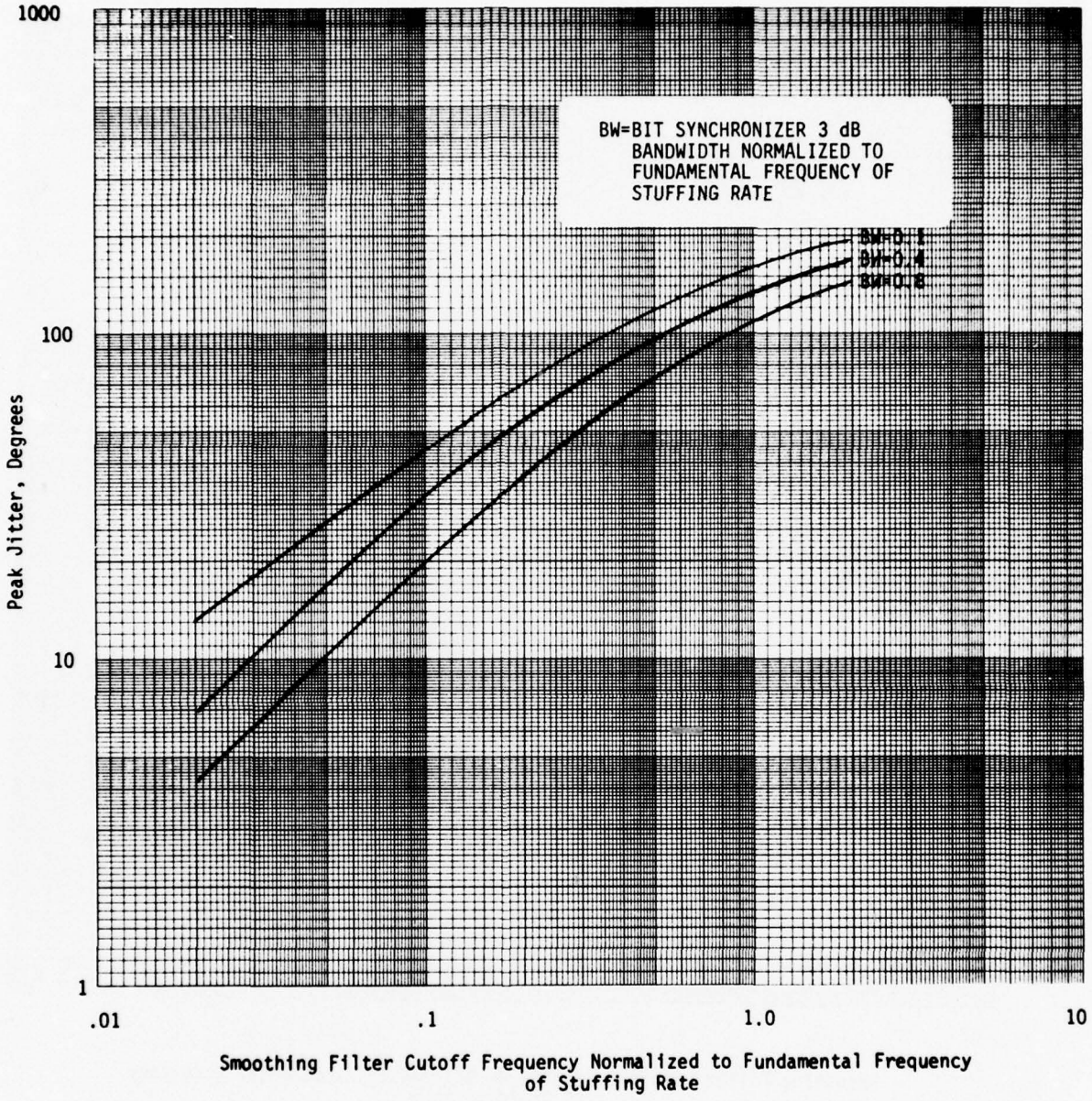


Figure 5.2-3. Effect of Second Order Bit Synchronizer Bandwidth on Peak Error Induced by Pulse Stuffing Jitter

5.3 Design Characteristics of First and Second Level Multiplexers

The bit synchronizer receiver design in the first level multiplexer establishes the criteria for phase jitter tolerance. The second level multiplexer design controls the amount of phase jitter. Obviously, both have many other requirements which must be traded off against jitter. Usually, the selection of the bit synchronizer bandwidth in the first level multiplexer results from a trade-off between narrow noise bandwidth requirements and a large tracking bandwidth requirement. The choice of second level multiplexers can be dictated by its application. A selection of a positive-negative second level multiplexer will be made if it is deemed necessary to have a data transport rate equal to the nominal channel rate. Supposedly, such an arrangement aids in the transition from what is basically a nonsynchronous system to a synchronous system. The selection of smoothing loop order is a matter of economy. A first order loop design would be more economical. However, narrow bandwidths in a first order loop require a large phase error to achieve the same offset frequency deviations in the VCO. Consequently, when a tributary input channel nominal frequency is different from the VCO's nominal frequency, a large phase error is required to offset the VCO to the tributary channel rate. The larger phase error implies a greater increase in the buffer size. Quantization requirements or phase error granularity cause a practical limitation on buffer size. Consequently, in light of narrower bandwidth requirements a second order loop becomes a natural choice to avoid this problem.

5.3.1 Selecting a Second Level Multiplexer

The tributary input frequency range is normally a design input for the second level multiplexer. From a jitter consideration the two variables to be selected are data transport frequency and number of bits per stuffing opportunity. In essence, the desired choice is to select a data transport frequency such that the offset frequency is large so that it can be filtered readily and the bits per stuffing opportunity low to generate the lowest possible waiting time jitter.

However, other constraints normally enter into the picture. A total data rate (channel bandwidth) limitation will place restraints on the use of a large data transport frequency and a large number of overhead bits (required to identify stuffing opportunities). In fact, for a fixed total data rate, there

is an optimum choice of data transport frequency and bits per stuffing opportunity for minimum total jitter for a given smoothing loop bandwidth.

The choice of one of four schemes considered in the past by industry has generally been narrowed to two schemes: positive stuffing and positive-zero-negative stuffing. Negative stuffing is generally not used. The fourth scheme (positive-negative stuffing) has been proposed but not implemented.

Positive stuffing gives the added degree of freedom of selecting a data transport frequency. This enables the designer to select a reasonable range of offset frequencies, where the stuffing jitter can be adequately filtered by the smoothing loop. A positive-zero-negative stuffing scheme does not allow the designer this degree of freedom. In order to remove the impact of stuffing jitter over the offset frequency range (which includes zero Hz), it becomes necessary to implement a very narrow bandwidth smoothing loop. The CCITT recommendations (Ref. 4) were strongly in favor of the fourth scheme as a solution to obtaining a system which has a data transport frequency equal to the nominal frequency and which avoids the problem of removing the impact of stuffing jitter. However, this scheme was not addressed during the course of this study and, consequently, no verification of the CCITT recommendations can be offered.

5.3.2 Selecting a Smoothing Loop

The smoothing loop's function is to remove the jitter introduced by the pulse stuffing operation and to retime the data to the original tributary input channel rate. Therefore, a narrow smoothing loop bandwidth is a desired feature. The limit on how narrow this smoothing loop bandwidth can be is dictated by the data bandwidth of the tributary input channel. However, such data slew rates are usually extremely narrow, so the bandwidth limit is dictated by the practicality of implementing narrower bandwidths.

The choices discussed for smoothing loop implementations are digital vs analog and first order vs second order. In the first trade-off, the digital loop design can provide narrower bandwidths and in addition, some amount of programming of ranges should it be desired. This fact emerged during our hardware simulator design phase. It was also obvious that neither approach would offer an overwhelming cost advantage. The digital frequency source - NCO (numerically controlled oscillator) has a source of jitter associated with the approach used in generating the frequency variation - pulse slicing. The

digital NCO approach has a greater resolution (capability) - lower K_o value - than is achievable by the analog approach. This is the reason that lower bandwidths can be achieved. In addition, the digital second order loop offers a fairly non-volatile Δf memory. Hybrid loops were not considered in this hardware implementation.

The choice of first order vs second order smoothing loop is first of all one of economics. A first order loop is more economical. However, in a first order loop the frequency difference between the VCO nominal frequency and the tributary input frequency (Δf) is maintained by a static error. This error, in radians, is computed by the equation

$$\theta_e = \frac{2\pi\Delta f}{\alpha} \quad \text{, where } \alpha \text{ is equal to } \omega_c.$$

Whence,

$$\theta_e = \frac{\Delta f}{2\pi f_c} \text{ bits} .$$

As this static error range gets larger, the ability to attain accurate resolution of phase error is impacted. Extended ranges require more quantization to maintain the same resolution. Loss of phase error resolution impairs attaining small phase detector gain values K_d. This restriction places a limit on the lower bandwidths for a first order loop. At this point it becomes necessary to select a second order loop.

A point of interest is that instability due to loop delay as a result of the extended phase detector range does not appear to be a factor. The exercise in Appendix D of the Design Plan (Ref. 13) shows that there is a large stability phase margin for the loop bandwidths in question.

5.3.3 Selecting a First Level Multiplexer Bit Synchronizer

Unlike the smoothing loop whose function is to smooth out jitter, the bit synchronizer is intended to track the incoming signal. Timing errors result in lower signal-to-noise ratios. A small phase error is desired and, therefore, considered to be the criteria for good tracking performance for this function. The first requirement is to avoid "velocity offset" Δf phase errors, consequently,

a second order loop is selected. The assumption is that the input contains no acceleration error (e.g. Doppler frequency change). In addition to the Δf error, it is necessary to track the signal variations accurately. This is accomplished by using a wide bandwidth in relationship to the distributary input signal bandwidth as was evident in Figure 5.2.

However, it is also a fact that output phase jitter increases as the noise-to-signal ratio increases. Phase error due to noise has fluctuating statistical properties and, consequently, noise peaks. No matter how small the noise RMS value, there is always the probability it can exceed the range of the phase detector. Because sufficiently large noise will greatly increase the probability of exceeding the range of the phase detector, it becomes necessary to hold the noise as small as possible. Other than possibly controlling noise sources impacting the signal, the only choice available to the designer is narrowing the loop bandwidth to reduce noise. Thus, there exists a trade-off between the noise requirements for narrower bandwidths and the tracking requirements for larger bandwidths.

The noise bandwidth for a second order loop is given by

$$B_L = \tfrac{1}{2}\,\omega_n\,(\zeta+\frac{1}{4\zeta}),$$

which yields the narrowest noise bandwidth for ζ=0.5. In addition, values of ζ less than 0.707 greatly increase the oscillatory nature of the loop response. The value ζ=0.707 gives the smallest steady-state phase error for the range of $\zeta \geq 0.707$ (Ref. 17). Thus, a value such as ζ=0.707 appears as a judicious choice for this loop. The selection of ω_n is then the subject of a trade-off between the noise-to-signal ratio and the tracking error.

SECTION 6.0

IN-PLANT TEST AND EVALUATION (PHASE II)

6.0 IN-PLANT TEST AND EVALUATION (PHASE II)

Phase II served as an operational evaluation phase for this study. The objectives of Phase II were four-fold:

- Validate the hardware simulator
- Obtain jitter data to enhance the understanding of jitter characteristics
- Compare results with those obtained during the analysis effort (Phase I) and interactively upgrade the overall study results.
- Develop and validate techniques for measurement of jitter in fielded equipment.

These four objectives were satisfactorily achieved during Phase II. An amenity of the testbed facility was the rapidity with which experiments could be accomplished. The hardware simulator is a real-time testbed; consequently, a large number of experiments were accomplished in the given Phase II Study time period. The hardware testbed experimental results provided credence to the analysis results.

6.1 Test and Evaluation Summary

The in-plant test and evaluation phase was conducted to obtain jitter data from the second level multiplexer simulator (SLMS) testbed. There are three second level multiplexer simulators in the testbed. Each simulator is composed of a jitter simulator, which models the effect of stuff/destuff actions of a multiplexer/demultiplexer pair, and a smoothing loop. The smoothing loop filtered the jitter induced by the pulse stuffing synchronization technique used in the second level multiplexers. The jitter simulator and smoothing loop parameters, the tributary input data stream, the output transport data stream, the number of data bits between stuffing opportunities and the bandwidth were varied during these tests. The effect of varying a particular parameter on jitter was tabulated by measuring the peak-to-peak and RMS values of jitter.

The test and evaluation phase consisted of the thirteen formal tests outlined in the test plan (Ref. 14). Some additional experimentation was conducted to verify specific subtle analysis points. In general, most of the tests were performed to observe jitter as a function of a particular parameter as is tacit from the preceding paragraph. The last test in the series (Test 13) deserves special mention since it served to determine the effects of jitter on the HN-74 E-CDS

Receive Unit. This unit, which receives the jittered output of a second level multiplexer simulator, was used as an input to a data generator. The output of the data generator excited the HN-74 E-CDS Receive Unit. This unit provided data and clock to an error detector unit. The data generator and error detector units were programmed to compare data streams for data integrity. The error detector unit measures average error rates. Thus, the susceptibility of the HN-74 to bit slips could be determined.

The data obtained from the testbed verified that the software simulation and hardware simulator produce similar results. There are several graphs in this Section which can be compared directly with the analysis results presented in Section 5.0. In particular, the data for jitter versus bandwidth in Subsection 5.1.2 obtained from MUXJIT and that obtained from the testbed in Subsection 6.4.1 compare favorably. Also, the prediction that there is no jitter accumulation from node to node is reinforced by the testbed results. In addition, a Duttweiler type curve was produced which compares favorably with the theoretical curve in Figure 5.1.1-1.

6.2 Test Matrix Description

In order to perform the pertinent experiments in a methodical manner, a test matrix was devised. The test matrix is given in Table 6.2. There are thirteen tests tabulated in the matrix. The first twelve tests are concerned with varying the jitter simulator and digital smoothing loop parameters to study the impact on the creation and accumulation of jitter. The last test, Test 13, looks at the effect of jitter on the E-CDS Receive Unit of the CY-104, a first level multiplexer.

The matrix tabulates the experimental control parameters and the measurement parameters involved in each of the thirteen experiments. There are seven control parameters and five measurement parameters. The control parameters establish the test set-up requirements and provide control over the variables of the simulation. As such they configure the specific model and condition being simulated. The measurement parameters established the data which had to be monitored. The matrix at a glance shows which experimental control parameters are fixed and which are the variables of the simulation for a given experiment.

To facilitate the discussion in the sequel of this Section and to explain the nomenclature in Table 6.2, Test 1 from Table 6.2 will be used as

Table 6.2. Test Matrix

	CONTROL PARAMETERS							MEASUREMENT PARAMETERS				
Test	Stuff Mode	Tandems	T1 MHz	T1S MHz	BPO	Delay	BW Hz	T1 MHz	T1S MHz	ρ	Jitter	BER
1. Smoothing Loop BW Impact on M12	+	1	1.544	1.5458	288	0	VAR	X	X	X	X	
2. Smoothing Loop BW Impact on T1-4000	+	1	1.544	1.544935	576	0	VAR	X	X	X	X	
3. BPO Impact on M12	+	1	1.544	1.5458	VAR	0	C	X	X	X	X	
4. BPO Impact on T1-4000	+	1	1.544	1.544935	VAR	0	C	X	X	X	X	
5. Smoothing Loop Impact on GSC-24 (NEG)	+/-	1	1.544	1.543638	889	0	VAR	X	X	X	X	
6. Impact of Cascading Two M12	+	2	1.544	1.5458	288	0	VAR	X	X	X	X	
7. Impact of Cascading Three M12	+	3	1.544	1.5458	288	0	VAR	X	X	X	X	
8. Impact of Cascading Two T1-4000	+	2	1.544	1.544935	576	0	VAR	X	X	X	X	
9. Impact of Cascading Three T1-4000	+	3	1.544	1.544935	576	0	VAR	X	X	X	X	
10. Impact of T1S Phases in Cascaded Network	+	3	1.544	1.5458	288	2,4,8, 12	C	X	X	X	X	
11. Impact of T1S Rate	+	1	1.544	VAR	288	0	C	X	X	X	X	
12. Impact of T1 Rate	+	1	1.544± 200 Hz	1.5458	288	0	C	X	X	X	X	
13. Jitter Impact on HN-74 BER	+	1	1.544	1.5458/ 1.544935	288/ 576	0	VAR	X	X	X	X	X

an example. The first column in Table 6.2 indicates the test number. The test stuff mode is denoted in column 2. It designates the pulse stuffing multiplexer category being simulated. The mode is either positive stuffing (+), negative stuffing (-), or positive-zero-negative stuffing (+/-). Test 1 indicates a positive stuffing exercise. Column 3 depicts the number of jitter simulator/smoothing loop pairs used in the experiment. For Test 1 only one second level multiplexer/demultiplexer simulator was employed.

The fourth column provides the input tributary data rate. For our example, Test 1, this rate was 1.544 Mbps. This was the input to the jitter simulator. The data transport rate was 1.5458 Mbps and is tabulated in column 5. This was a simulation of the data transport rate digit stream for one channel out of the multiplexer and into a demultiplexer.

The number of bits per opportunity, or stuffing interval, for Test 1 is given in column 6. There were 288 data bits which had to be transmitted before a stuffing opportunity was available.

Column 7 is required to simulate the real world phenomenon that the data transport clocks (T1S clocks) in a tandem fielded network do not have the same phase. Each clock is generated by a separate oscillator. To model the phenomenon, delay circuitry was implemented in each jitter simulator. The delay circuitry provided the capability of changing the data transport rate phase in 16 discrete steps. Selection of the phase was determined by dip switches located on the jitter simulator cards. For Test 1 the delay was set to zero.

The bandwidth designation in Column 8 implies whether a constant (C) bandwidth was being maintained during the experiment or the bandwidth was being varied (VAR). For experiment 1 the bandwidth was varied. The values over which the bandwidth was varied are listed in the data sheets in Appendix C.

Going from the experimentally controlled parameters to measurement parameters, T1 and T1S in columns 9 and 10, respectively, have the same definition as T1 and T1S in columns 4 and 5, respectively. The stuffing ratio in column 11 had to be measured in Test 1 along with the RMS and peak-to-peak jitter. An 'X' designates a measurement, or measurements, had to be made for that parameter. For this case the bandwidth was varied, and the RMS and peak-to-peak jitter were tabulated.

The last column, column 13, designates whether a Bit Error Rate (BER) measurement was made. Only in Test 13 BER measurements had to be made. In this test it was desired to determine the effects of jitter on the HN-74 E-CDS Receive Unit.

The twelve 'jitter' experiments tabulated in Table 6.2 were performed. The first two were variable bandwidth experiments employing Bell M12 and VICOM T1-4000 parameters. By varying the bandwidth of the smoothing loop, the effect on jitter could be ascertained. Experiments 3 and 4 looked at the effect of changing the stuffing ratio on jitter for the Bell M12 and VICOM T1-4000. Test 5 dealt with the Martin-Marietta AN/GSC-24 parameters for positive-zero-negative stuffing. Here, again, the bandwidth was varied.

Experiments 6 and 7 looked at jitter for two and three nodes in tandem, respectively, and are an extension of experiment 1. The same can be said for tests 8 and 9 which are an extension of test 2. Here the output jitter for two and three multiplexer/demultiplexer pairs in tandem were measured.

Experiment 10 looked at three jitter simulator/smoothing loop pairs in tandem. The phase of the data transport clock was varied in this experiment. The delays employed corresponded to 1/8, 1/4, 1/2 and 3/4 of a 2π period. The RMS and peak-to-peak jitter were measured to determine the effect of clock delay.

Test 11 looked at jitter when the transport rate was varied for the Bell M12 case. The last experiment, Test 12, in the 'jitter' series varied the input offset rate ±200 Hz.

The final experiment (Test 13) in the test matrix was concerned with the effects of jitter on the HN-74 E-CDS Receive Unit. Two values of the output data transport rate were used along with bandwidth variation. The purpose of this experiment was to determine how jitter effects the bit sync circuit of the E-CDS Receive Unit. It was desired to measure the average error rate occurring in the data output stream of the receive unit over a period of time.

6.3 Test Setup and Configuration

To perform the experiments tabulated in the test matrix, the test setups given in Figure 6.3-1 and Figure 6.3-2 were utilized. The instrumentation test configuration shown in Figure 6.3-1 was employed to carry out tests one through twelve in the test matrix. The test setup in Figure 6.3-2 was employed to carry out test 13 in the test matrix. As pointed out previously, this latter test gathered BER data when the bit timing recovery circuit of the E-CDS Receive Unit of the HN-74 was stressed with jittered data.

As can be seen from Figure 6.3-1, the test setup consisted of the jitter simulator test fixture, which also contained the smoothing loops, two frequency synthesizers, two oscilloscopes for observing waveforms, a counter

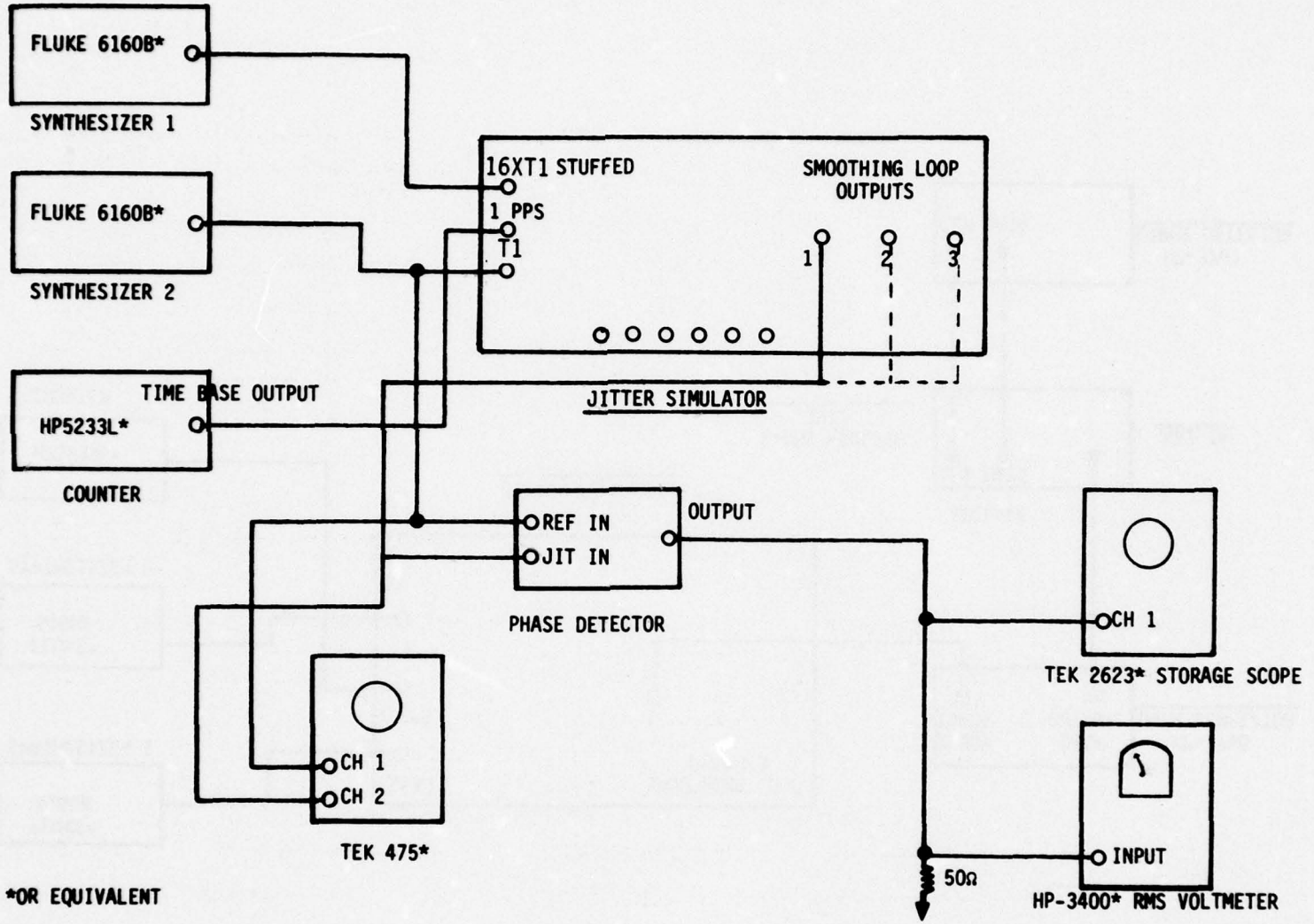


Figure 6.3-1. Test Setup for Measurement of 2nd Level Multiplexer/Demultiplexer Simulator Output Phase Jitter

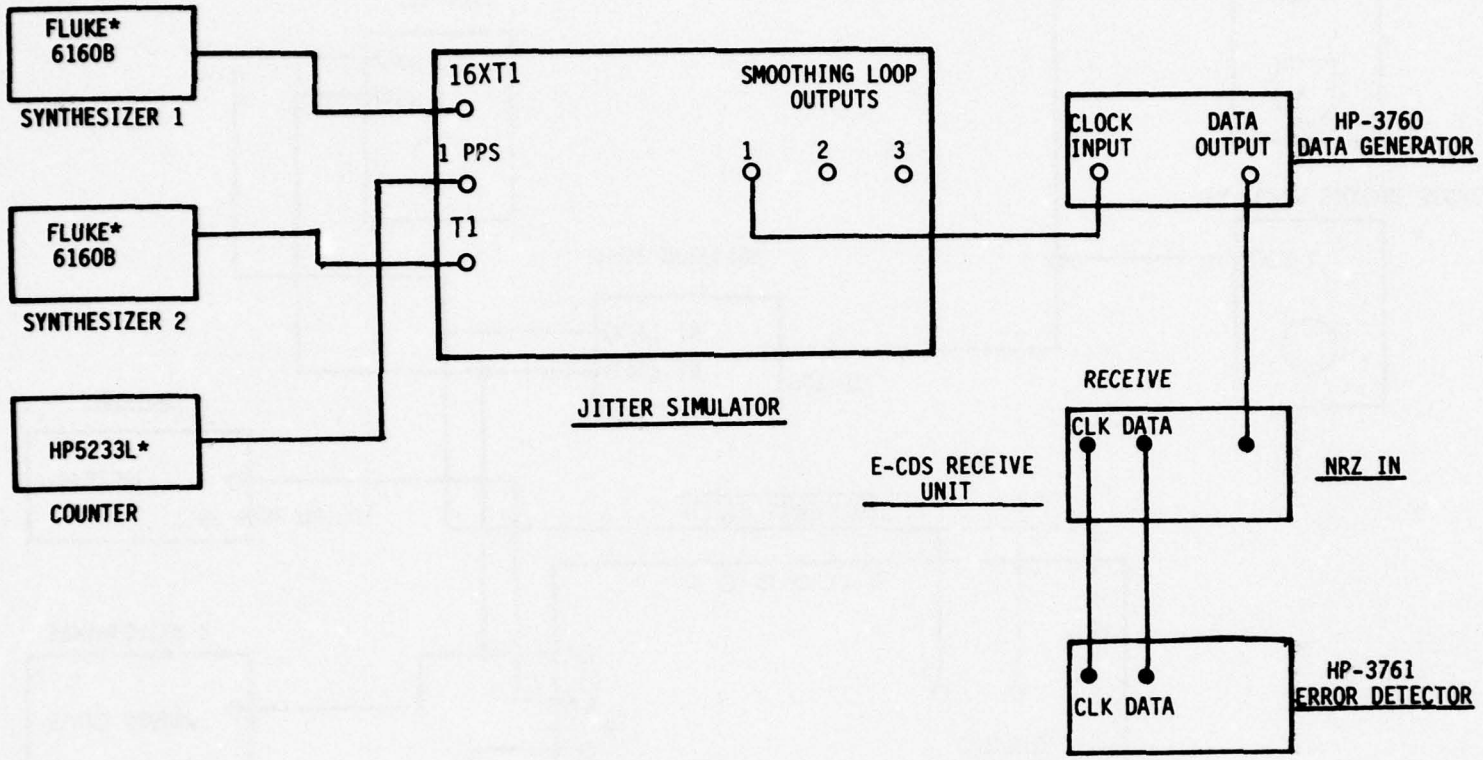


Figure 6.3-2. Test Setup for 1st Level Multiplexer
Bit Error Rate Measurement

which delivered one pulse per second to the jitter simulator, an RMS voltmeter, and a special phase detector test fixture. Synthesizer 1 delivered a 24-25 MHz signal to the simulator. This signal was counted down and employed as the simulator clock. It also served as the digit transport signal, T1S, in the simulator. Synthesizer 2 supplied the input tributary clock. One pulse per second was outputted to the jitter simulator from the time base output counter. This pulse updated the actual stuffs and stuff opportunities displays on the jitter simulator as shown in Figure 6.3-3. The dual trace scope in the lower left area of Figure 6.3-1 displayed the jittered signal and the T1 reference signal for convenient comparisons. The jittered waveform could be observed jittering with respect to the T1 stable reference signal.

The T1 stable reference signal and the jittered output signal were fed into a phase detector test fixture designed specifically for this study. The phase detector measured the difference between the T1 stable reference signal (1.544 Mbps) and the smoothed jittered clock out of the testbed. This was accomplished by integration between the positive edge of the T1 signal and the positive edge of the smoothed jittered signal. The integrated value was sent to a sample and hold circuit. The output of the sample and hold circuit was displayed on an oscilloscope to provide a display of the phase variation of the jittered waveform.

The dotted lines on the jitter simulator in Figure 6.3-1 represent experiments for tandem measurements. For example, smoothing loop output 2 represents the jittered output from the second jitter/smoothing loop pair in tandem.

Figure 6.3-2 represents the configuration for test 13. The output of the smoothing loop is used to supply a bit rate clock to the HP 3760A Data Generator. The data generator has the capability of producing selected digital words and pseudorandom binary sequences. The output of the data generator supplies NRZ data for the HN-74 E-CDS Receive Unit. The output of the HN-74 E-CDS Receive Unit is then checked for errors by the HP 3761A Error Detector. This error detector has been specifically designed for operation with pseudorandom sequences produced by the HP 3760A Data Generator. It receives data and clock from the HN-74 E-CDS Receive Unit and performs error detection using bit by bit comparison with an internally generated closed loop reference sequence.

The BER measurement is computed from more than 100 errors and has a range of 9.9×10^{-1} to 0.1×10^{-9}.

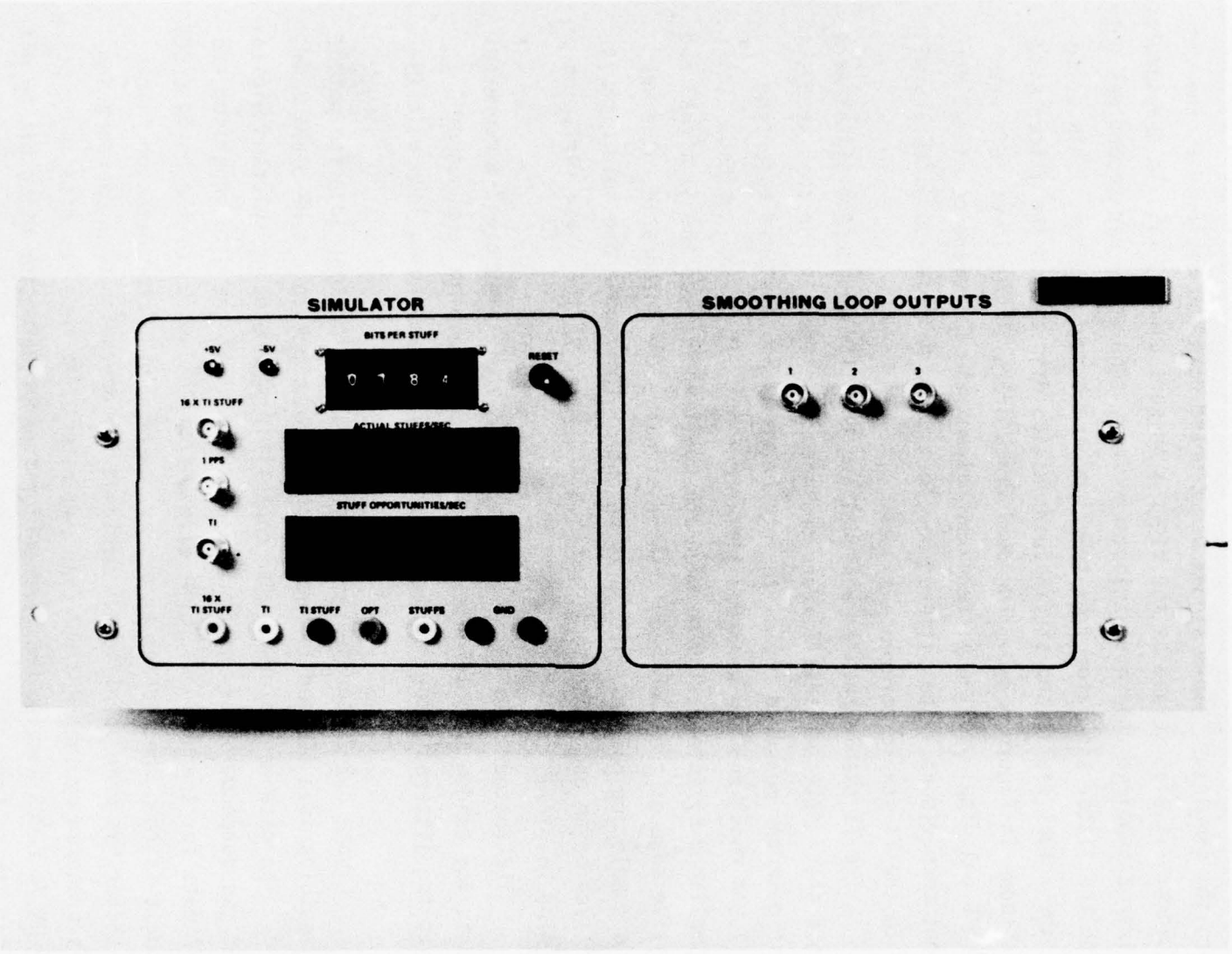


Figure 6.3-3. Jitter Simulator Front Panel

6.4 Evaluation of Test Results

The results of the thirteen formal experiments specified in the test plan and conducted during the test and evaluation effort are described in this subsection. Because of the nature of the thirteen experiments, their results can best be presented in eight distinct categories.

- Effect of varying smoothing loop bandwidth while using positive stuffing
- Effect of varying bits per opportunity (BPO)
- Effect of varying smoothing loop bandwidth while using negative stuffing
- Effect of tandem configurations
- Effect of varying data transport rate phase angle
- Effect of varying data transport rate
- Effect of jitter on the E-CDS Receive Unit

The evaluation of the experimental results are discussed in the following eight subsections using the above categories. The specific test results are contained in Appendix C under Tables C-1 through C-15.

6.4.1 Effects on Jitter by Varying Smoothing Loop Bandwidth for Bell M12 and VICOM T1-4000 Parameters (Tests 1 and 2)

The test objective for experiments 1 and 2 of the test matrix in Table 6.2 was to determine jitter effects by varying the bandwidth cutoff frequency of the smoothing loop. The fixed experiment control parameters are given in Table 6.2, and the variable control parameters are provided in Appendix C, Table C-1 for the Bell M12 parameters and Table C-3 for the VICOM T1-4000 parameters. Appendix C contains the data sheets for all the tests in the test and evaluation phase of this study. Table C-2 and Table C-4 in Appendix C contain the raw data for the Bell M12 parameters and VICOM T1-4000 parameters, respectively. These data consist of the phase measurements from the special phase detector test fixture described in Subsection 6.3.

Graphs of RMS jitter and peak-to-peak jitter versus bandwidth are provided in Figures 6.4.1-1 and 6.4.1-2, respectively. As can be observed, data for both the Bell M12 and VICOM T1-4000 have been plotted. For both cases it can be seen from the graphs that as the bandwidth decreases so does the jitter. This was to be expected as pointed out earlier in Section 5 which discussed

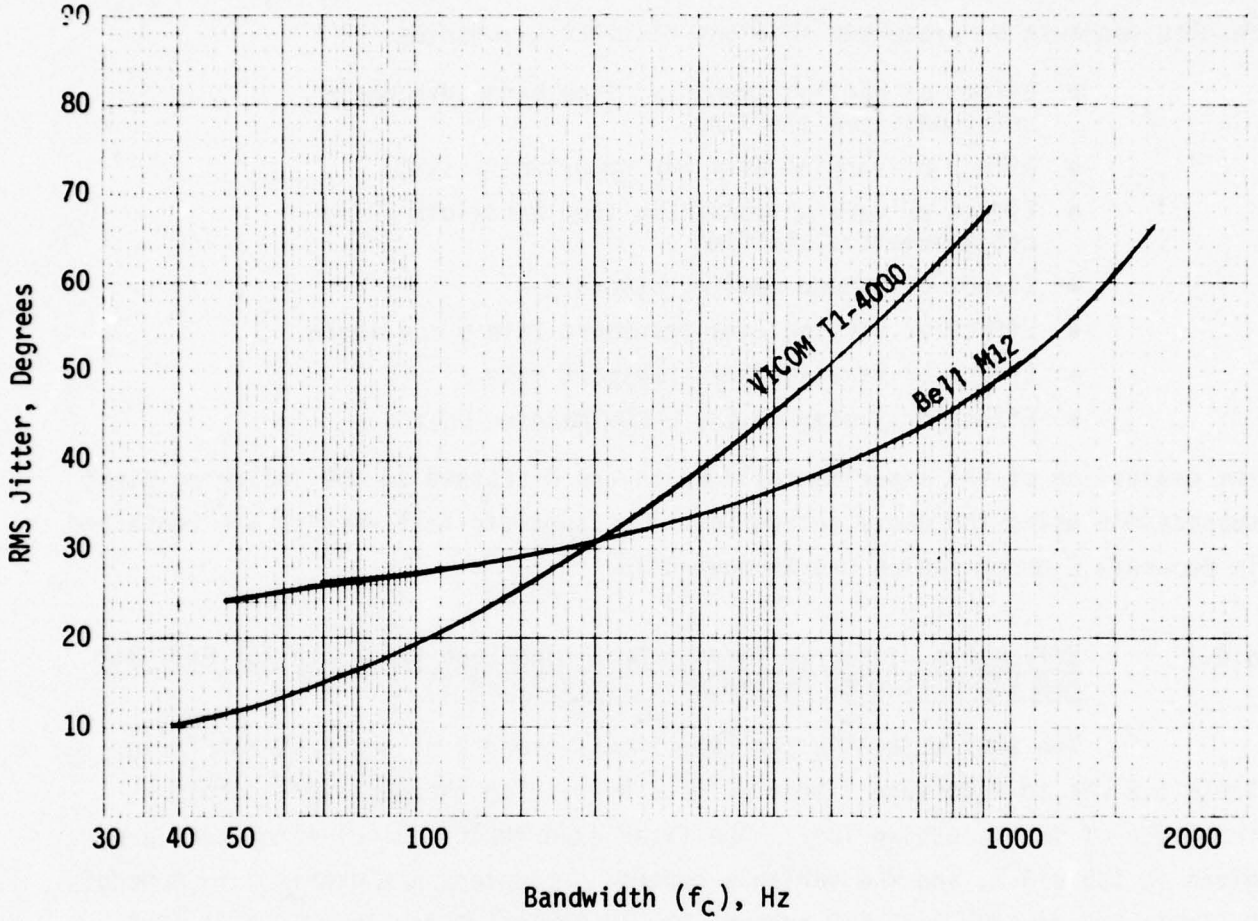


Figure 6.4.1-1. RMS Jitter Versus Bandwidth (f_c) for the Bell M12 and VICOM T1-4000 of Test 1 and Test 2, Respectively, in the Test Matrix

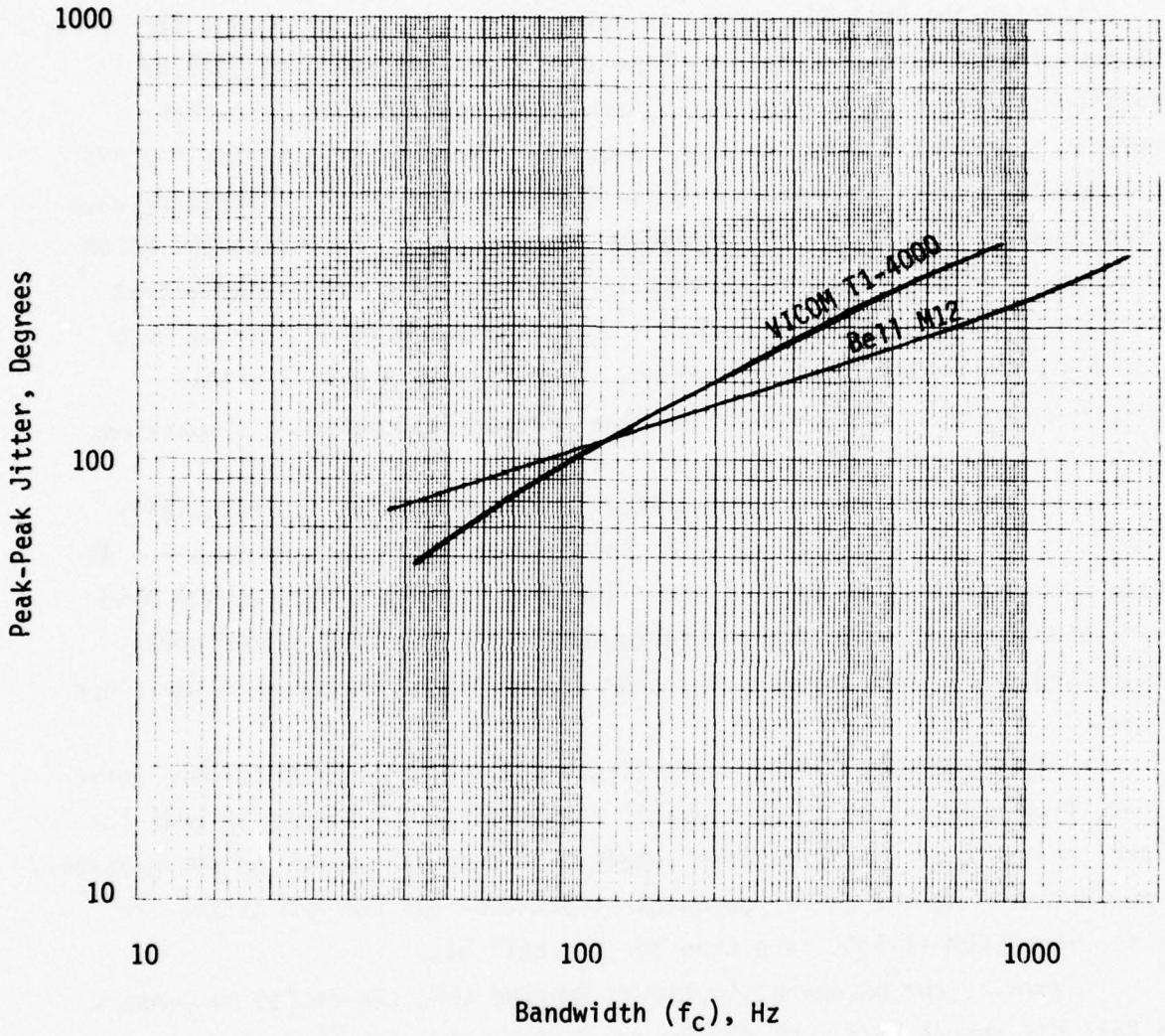


Figure 6.4.1-2. Peak-Peak Jitter Versus Bandwidth (f_c) for Bell M12 and VICOM T1-4000 of Test 1 and Test 2, Respectively, in the Test Matrix

Phase-I analysis results. Narrowband filters improve the jitter performance of the multiplexer/demultiplexer devices.

An interesting comparison can be made between Figure 5.1.2-7 and Figure 6.4.1-1. Figure 5.1.2-7 was obtained with the software simulation MUXJIT. Comparing the Bell M12 curves in both graphs, it is noted that at 100 Hz bandwidth the curves deviate by less than three degrees. At 1000 Hz the variation is less than one degree. Overall the variation is less than four degrees. Considering the transient problems incurred in obtaining the RMS values in MUXJIT and the resolution problem that occurred in the laboratory when taking readings off the scope, the agreement is very good. Comparing the VICOM T1-4000 curve in Figure 6.4.1-1 with that in Figure 5.2.1-7, it is noted that the curves are similar. It is seen that the two curves do not differ by more than four degrees. As was commented above, these results are well within experimental accuracy. This implies that the hardware and software simulations agree very well with each other.

The graph of peak-to-peak jitter in Figure 6.4.1-2 is essentially a straight line for the Bell M12 curve on logarithmic paper. There is a 6.4 dB per decade change in peak-to-peak jitter. The plot for RMS jitter versus bandwidth indicates that as bandwidth increases more pulse stuffing jitter energy is being passed. This becomes apparent from the monotonic increase in the slope of the curve.

Unlike the Bell M12 curve in Figure 6.4.1-2, the VICOM T1-4000 curve in the same figure is not quite as linear. Furthermore, the change in peak-to-peak jitter per unit of smoothing loop cutoff frequency is greater by approximately 3.6 dB per decade. At the higher bandwidths, peak-to-peak and RMS jitter are greater for the VICOM T1-4000 case than for the Bell M12.

Overall, the hardware simulation implied that the design parameters for the Bell M12 result in a much flatter characteristic with less of a slope than for VICOM T1-4000.

6.4.2 Effects on Jitter by Varying the Bits Per Opportunity Between Stuffs for Bell M12 and VICOM T1-4000 Parameters (Tests 3 and 4)

The purpose of these tests were to determine the effects on jitter by changing the number of data bits that occurred between stuffing opportunities. By varying this parameter, the stuffing ratio, ρ, was controlled. The stuffing ratio was accorded the range from .1 to .9. This particular discussion encompasses

Test 3 and Test 4 in the test matrix of Table 6.2. For the Bell M12 the test data occur in Table C-5 of Appendix C. The data for the VICOM T1-4000 are tabulated in Table C-6.

The results of this experiment are portrayed in Figure 6.4.2-1 through Figure 6.4.2-4. The first two figures in this series plot RMS jitter versus stuffing ratio. The last two figures consider peak to peak jitter versus stuffing ratio.

There is a very interesting phenomenon that is apparent from the graphs. As the stuffing ratio is increased, the curves have an underlying increasing secular trend. Comparing Figure 6.4.2-1 and Figure 6.4.2-2 with the Duttweiler curve in Figure 5.1.1-1, several comments can be made. First, the theoretical graph in Figure 5.1.1-1 is symmetrical about ρ=0.5. The test curves attempt to be symmetrical; however, the underlying secular trend biased the curves upward. The major peaks of Figure 6.4.2-1 and Figure 6.4.2-2 occur at the same abscissa points as for the curve in Figure 5.1.1-1. Another point is that there is greater correlation between the theoretical curve and the experimental curve in those areas where the higher peaks occur. The relative amplitude of a minor peak with respect to the major peak is not as reliable as the peaks decrease in size. The final comment is that the left half ($\rho \leq .5$) of the experimental curves appear to correlate better with their theoretical curve counter part.

For these experiments the stuffing ratio was varied by incrementing the BPO from 86 bps to 773 bps for the Bell M12 case and from 165 bps to 1487 bps for the VICOM T1-4000 case. Recall from the general discussion in Subsection 4.1.1 and for Figure 4.1.1-3, in particular, that for a constant offset frequency, the waiting time jitter amplitude increases as the stuffing opportunity rate, f_s=T1S/BPO, decreases. For the Bell M12 and the VICOM T1-4000, the constant offset frequencies are 1800 bps and 935 bps, respectively, and T1S is fixed in Table 6.2. As the bits per opportunity were increased, the magnitude of the waiting time jitter was increased. Therefore, more jitter energy was introduced and, hence, passed through the filter. This is the reason for the underlying upward secular trend for the graphs in Figures 6.4.2-1 through 6.4.2-4. Note that this effect is more apparent in the peak-tc-peak graphs than the RMS graphs because of the averaging effect of the RMS voltmeter.

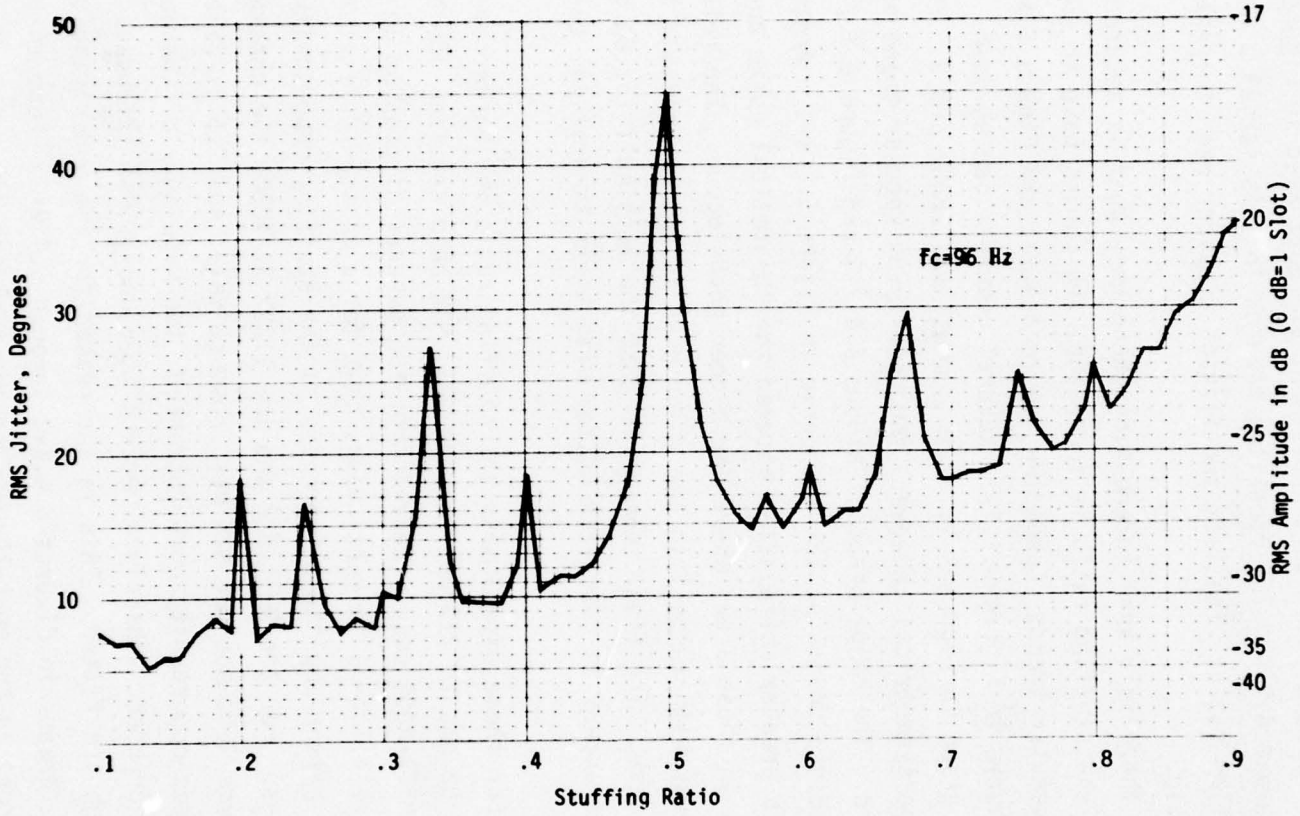


Figure 6.4.2-1. RMS Jitter Versus Stuffing Ratio (ρ) for the Bell M12 for Test 3 in the Test Matrix

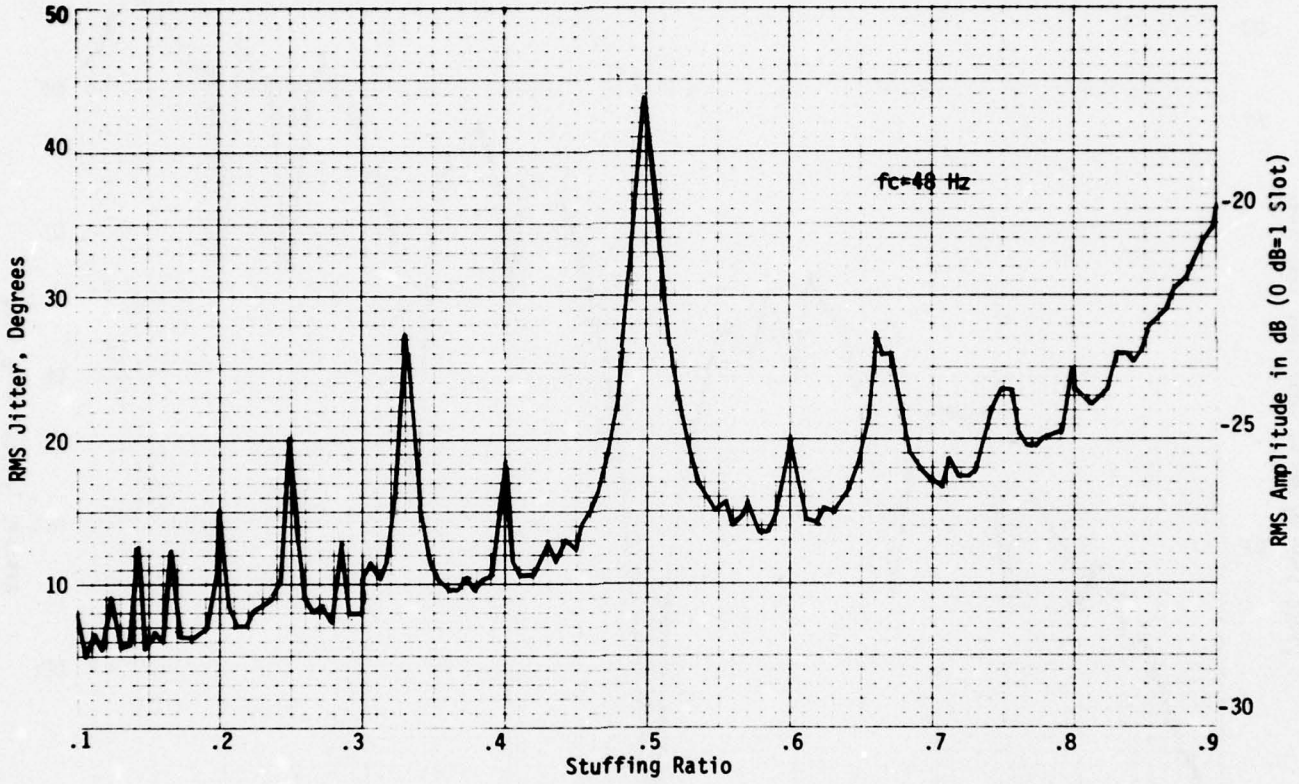


Figure 6.4.2-2. RMS Jitter Versus Stuffing Ratio (ρ) for the VICOM T1-4000 for Test 4 in the Test Matrix

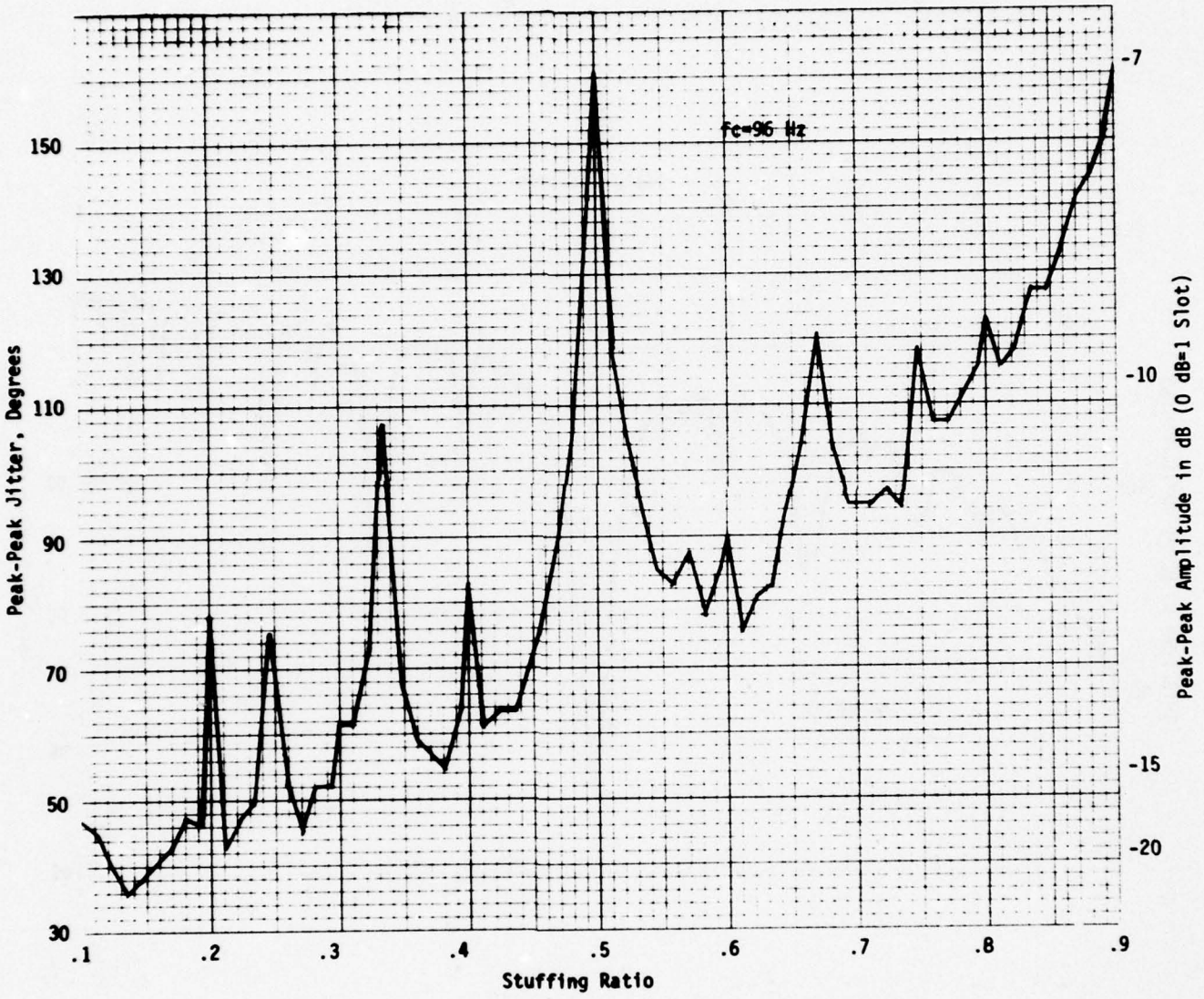


Figure 6.4.2-3. Peak-Peak Jitter Versus Stuffing Ratio (ρ) for the Bell M12 for Test 3 in the Test Matrix

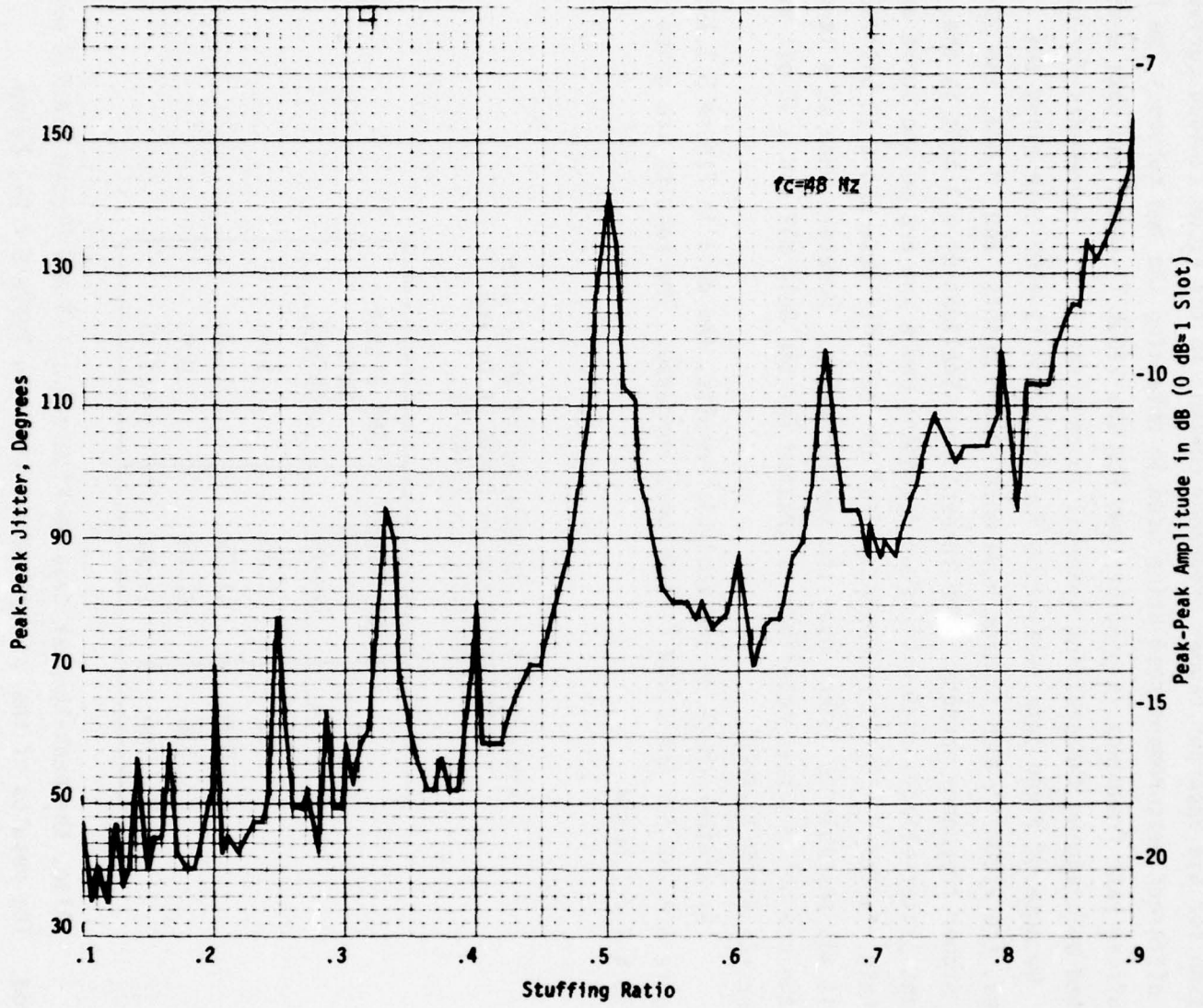


Figure 6.4.2-4. Peak-Peak Jitter Versus Stuffing Ratio (ρ) for the VICOM T1-4000 for Test 4 in the Test Matrix

Note that the graph in Figure 6.4.2-4 has narrower peaks than the graph in Figure 6.4.2-3. This implies that the curve has a power spectral density which has a greater share of its total energy distributed in the higher frequencies. One reason for the apparent higher frequency content in the VICOM T1-4000 curves was due to different measurement resolution used in obtaining the two curves. The Bell M12 stuffing rate frequency is greater than for the VICOM T1-4000, and data were collected by stepping the stuffing interval in constant 10 bit increments for both cases. Because of finer data resolution for the VICOM T1-4000 case along the abscissa, the VICOM T1-4000 figures have more sample points, and, hence, the apparent higher frequency content. One interesting sidelight of all this is the different jitter effects that will occur depending where you are on the curve and what 'gain' factor f_o=T1S-T1 represents. For the Bell M12 case and a 10 bit increment, it was possible to 'step' over the smaller peaks. However, when at a large peak, the change in jitter magnitude is greater for the Bell M12 and a 10 bit step than for the VICOM T1-4000.

As another check on the analysis results, the data in Figure 5.1.1-2 and Figure 6.4.2-2 for the VICOM T1-4000 were compared. The results are given in Table 6.4.2-1 below.

Table 6.4.2-1. Comparison of RMS Jitter for MUXJIT Using an f_c=46.75 Hz and SLMS Using an f_c=48 Hz.

Stuffing Ratio	RMS Jitter MUXJIT Degrees	RMS Jitter SLMS Degrees
.172	6.25	6.4
.350	11.75	11.0
.530	22.85	18.9
.700	17.75	17.3

Also, the peak-to-peak data in Figure 5.1.1-3 and Figure 6.4.2-4 were compared. The results of the comparison are given in Table 6.4.2-2 below.

It is noted that the RMS jitter data compares very well. The peak-to-peak jitter does not compare as closely; however, the general trend is there. Three reasons for this moderate deviation are the following:

Table 6.4.2-2. Comparison of Peak-Peak Jitter for MUXJIT Using an f_c=46.75 Hz and SLMS Using an f_c=48 Hz

Stuffing Ratio	P-P Jitter MUXJIT Degrees	P-P Jitter SLMS Degrees
.172	33.5	42.6
.350	55.1	58.0
.530	107.8	94.6
.700	106.4	92.2

1. For a small incremental change (.01) in stuffing ratio, depending upon where you are at on the curve, there can be a large change in jitter.
2. It was much more difficult to read the peak-to-peak voltage off an oscilloscope than from an RMS voltmeter.
3. Slightly different smoothing loop bandwidths were employed.

In summarization, it appears that the data obtained from the software simulation compared favorably with the hardware simulation data, and the hardware simulation results confirm the theories layed out in Section 4.0.

6.4.3 Effects on Jitter by Varying Smoothing Loop Bandwidth for AN/GSC-24 Parameters and a Negative Stuffing Mode (Test 5)

The purpose of this experiment was to operate in a negative stuffing mode, determine the effects on jitter by changing smoothing loop bandwidth, and to compare jitter results with those obtained in the analysis. The data for experiment 5 in the test matrix are tabulated in Table C-7 in Appendix C. Negative stuffing is denoted by the fact that T1S<T1.

Curves of RMS and peak-to-peak jitter versus bandwidth are given in Figure 6.4.3-1 and Figure 6.4.3-2, respectively. Like the Bell M12 in Figure 6.4.1-2, the plot for peak-to-peak jitter in Figure 6.4.3-2 exhibits a flatter characteristic for narrow bandwidths. The slope is 13.5 dB per decade. This is twice the slope of the Bell M12 case in Subsection 6.4.1. Therefore, for the AN/GSC-24 and the present parameters under discussion, changing the bandwidth by a given amount will produce a greater change in jitter for the AN/GSC-24 than

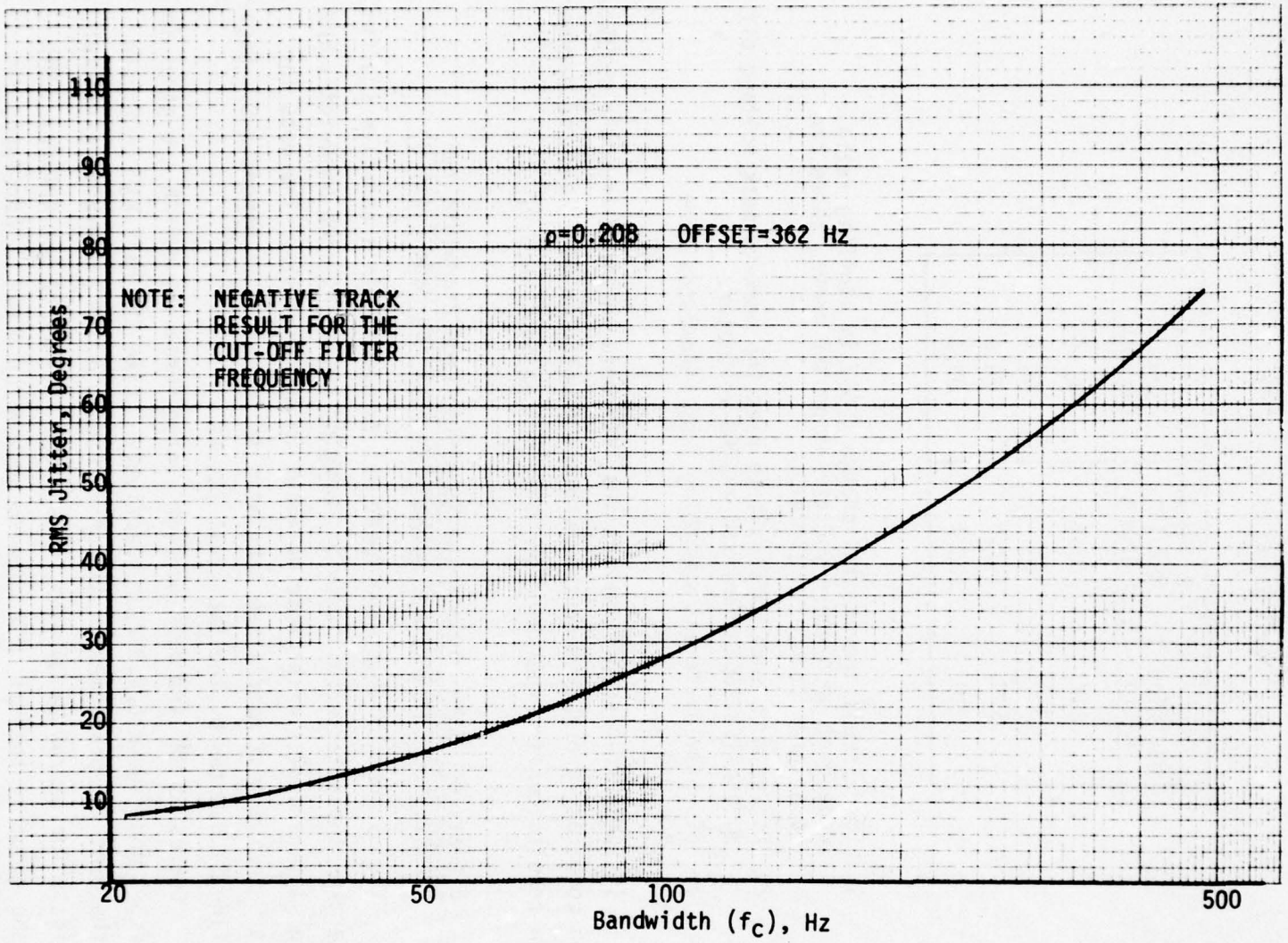


Figure 6.4.3-1. RMS Jitter Versus Bandwidth (f_c) for the AN/GSC-24 of Test 5 in the Test Matrix

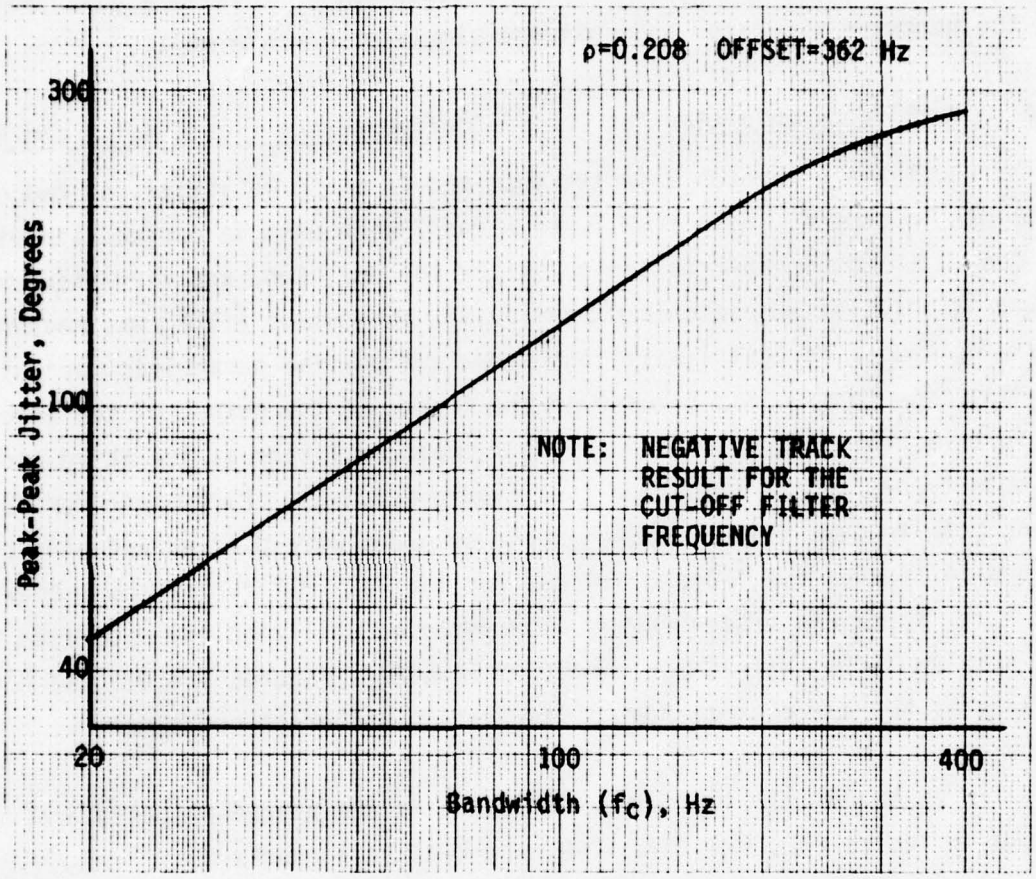


Figure 6.4.3-2. Peak-Peak Jitter Versus Bandwidth (f_C) for the AN/GSC-24 of Test 5 in the Test Matrix

for the Bell M12. However, note that the magnitude of the peak-to-peak jitter for the AN/GSC-24 test case is much less than for the Bell M12 to begin with. Because of the complexity of the AN/GSC-24, generalizations such as those made above should be applied with caution to fielded equipment in an operational environment.

Comparing Figure 6.4.3-1 with Figure 5.1.2-8, which was derived from MUXJIT in the analysis task, they compare quite well. This is a good indication that the hardware simulator and software simulator operate well.

6.4.4 Effects on Jitter for Tandem Configurations (Tests 6,7,8 and 9)

Tests 6 through 9 in the test matrix measured jitter for two or more simulators in tandem. Data from Tests 6 and 7 were used in conjunction with that from Test 1 to obtain information on jitter for one, two, and three tandem node configurations. As was described previously, the output jitter was measured for a single node in Test 1 while the bandwidth was the parametric variant for Bell M12 parameters. Test 6 measured the jitter at the output of the second node for the Bell M12 parameters. Test 7 measured jitter at the third smoothing loop output port of the simulator (see Figure 6.3.1-1). Parametric curves of RMS and peak-to-peak jitter versus number of nodes were plotted and have been provided in Figures 6.4.4-1 and 6.4.4-2 for the Bell M12 for various bandwidths.

The above procedure was also employed utilizing the data from tests 8 and 9, along with test 2, for the VICOM T1-4000. Figures 6.4.4-3 and 6.4.4-4 are plots of RMS and peak-to-peak jitter versus number of nodes for the VICOM T1-4000.

Data for all the curves discussed in the preceding paragraphs can be found in Tables C-2, C-4, C-8, C-9, and C-11 in Appendix C.

Looking at Figures 6.4.4-1 and 6.4.4-3 for RMS jitter, it is observed that the characteristics are essentially flat. The variation is two degrees or less for all curves except f_c=48 Hz in Figure 6.4.4-1. However, fitting a least squares straight line to the data would yield a negligible negative slope. Comparing this with the discussion in Subsection 5.1.3 and observing Figures 5.1.3-1 and 5.1.3-2, it appears that the hardware results are in line with the analysis results.

Looking at Figures 6.4.4-2 and 6.4.4-4 for peak-to-peak jitter, the curves are again essentially flat. The maximum deviation from zero slope along a curve is greater than for its RMS counterpart. The peak-to-peak values were

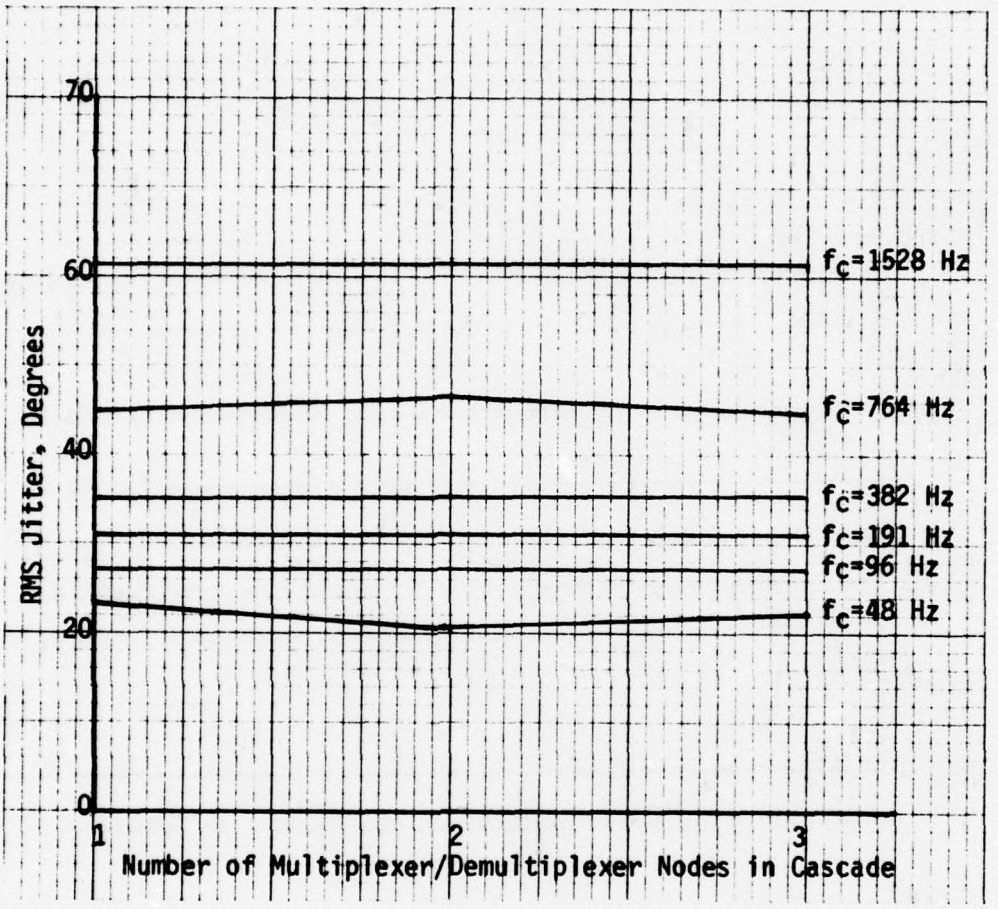


Figure 6.4.4-1. RMS Jitter Versus Number of Nodes for Bell M12 for Tests 1, 6, and 7 in the Test Matrix

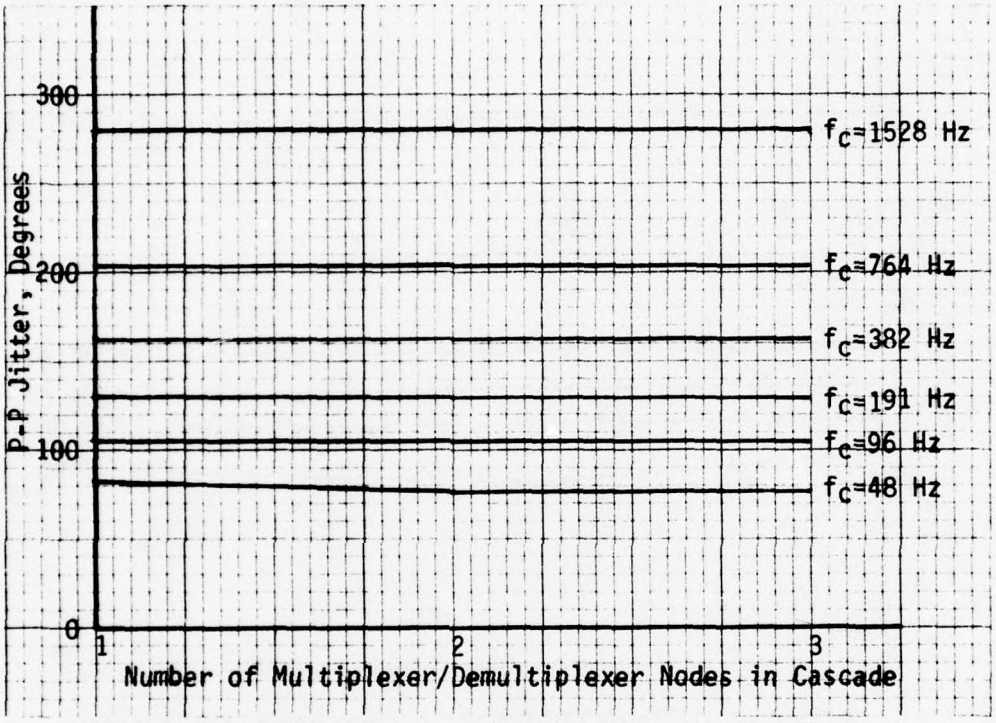


Figure 6.4.4-2. Peak-Peak Jitter Versus Number of Nodes for Bell M12 for Tests 1, 6, and 7 in the Text Matrix

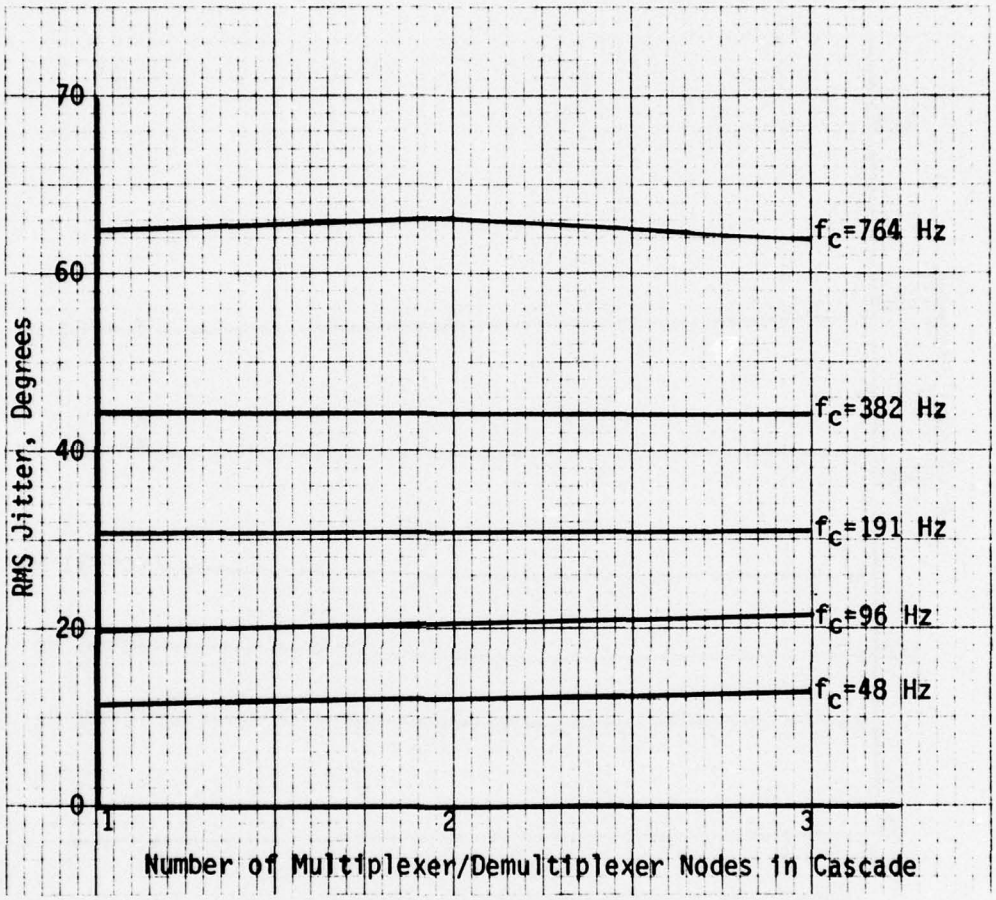


Figure 6.4.4-3. RMS Jitter Versus Number of Nodes for VICOM T1-4000 for Tests 2, 8, and 9 in the Test Matrix

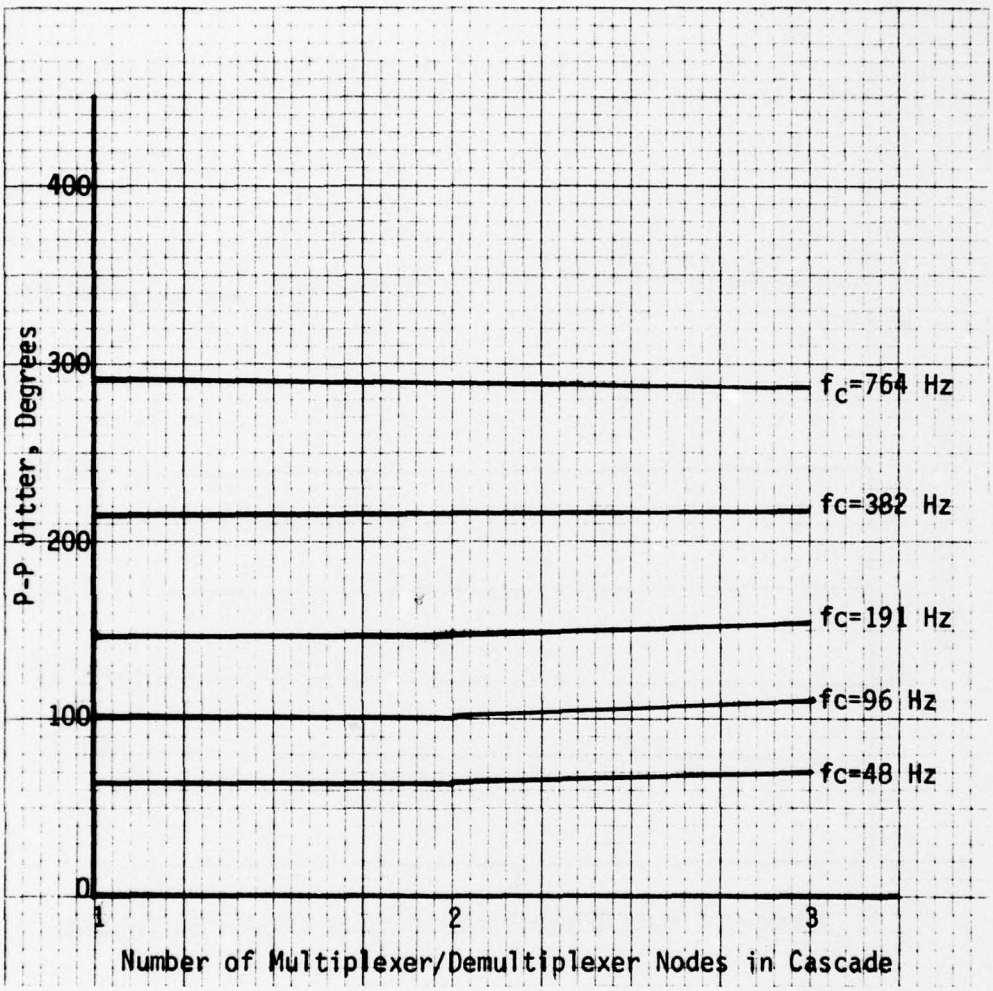


Figure 6.4.4-4. Peak-Peak Jitter Versus Number of Nodes for VICOM T1-4000 for Tests 2, 8, and 9 in the Test Matrix

more difficult to measure and did have a tendency to deviate more from the mean. However, there is no indication with the present collected data that the peak-to-peak jitter is increasing with the number of nodes. If there is an increase, it is within the resolution of the instrumentation.

6.4.5 Effects on Jitter When Varying Data Transport Rate Phase Angle (Test 10)

This experiment can be segmented into two parts. Test 10 in the test matrix was exercised maintaining all the data transport oscillator clocks at a constant phase and randomly selecting the clock phases.

6.4.5.1 Constant Phase Angle for All Nodes

The data transport digit stream's phase angle was varied for a single node and for three nodes in tandem. The phase angle, which represented the initial phase of the data clock, was varied through delays of 45^{o} (2), 90^{o} (4), 180^{o} (8), and 270^{o} (12) for all nodes in tandem; i.e., each node in tandem had the same phase delay.

RMS and peak-to-peak data were collected for a single node and for three nodes in tandem. The jitter was measured at the output of the last node in the tandem network. Data for this experiment can be found in Table C-12 of Appendix C. As can be observed, there was not much change in RMS, or peak-to-peak, jitter between delay steps and between measurements at the output of the first node and the last node. For this test configuration, it was concluded that a non-zero phase angle for the data transport digit stream clocking oscillator does not impact jitter. In fact, the greatest change of 2.3^{o} occurred in the peak-to-peak measurements. This value was not large enough to indicate a trend.

6.4.5.2 Variable Phase Angles for Three Node Tandem Configurations

For this segment of the experiment, three nodes in tandem were employed. Each node had a different phase angle for the data transport clock. Steps 9 through 11 in Table C-12 have phase angles of 45^{o} (2), 180^{o} (8), and 90^{o} (4) for nodes 1, 2, and 3, respectively. Steps 12 through 14 have phase angles of 0^{o} (0), 45^{o} (2), and 225^{o} (10) for nodes 1, 2, and 3, respectively. Finally, Steps 15 through 17 have delays of 225^{o} (10), 45^{o} (2), and 0^{o} (0) for nodes 1, 2, and 3, respectively.

From the data in Table C-12, there appears to be no drastic change in jitter. Hence, this is a strong indication that for tandem fielded configurations, where the phase angles are random, jitter will not be impacted.

6.4.6 Effects on Jitter When Varying the Data Transport Digit Rate (Test 11)

In experiment 11, the stuffing ratio, ρ, was controlled by varying the data transport rate and keeping the tributary input channel rate constant. The numerator of ρ is equal to f_o=T1S-T1, which is the offset frequency. The denominator of ρ is equal to f_s=T1S/BPO, which is the stuffing opportunity rate. For this experiment, f_s changed by less than .3% between ρ=.1 and ρ=.9. The stuffing ratio was essentially controlled by f_o for this experiment.

There are some similarities between this experiment and Duttweiler's analysis, which generated the theoretical curve in Figure 5.1.1-1. Duttweiler controlled the stuffing ratio by varying T1, the tributary input channel; since f_s is constant, f_o is the controlling variable.

Because of these experimental setup similarities, the data from Table C-13 in the Appendix yielded Figures 6.4.6-1 and 6.4.6-2, which look similar to the Duttweiler curve. Just as for Figures 6.4.2-1 through 6.4.2-4, the peaks occur at the proper locations on the abscissa. However, unlike Figures 6.4.2-1 through 6.4.2-4, there is no major upward secular trend. Also, the relative amplitude differences between the major peak and minor peaks in Figure 6.4.6-1 correlate better with those in Figure 5.1.1-1 than do those in Figures 6.4.2-1 and 6.4.2-2.

The reason for lack of an upward secular trend for the graphs in this subsection can be seen from Figure 4.1.1-2 and Figure 4.1.1-3. First, as mentioned above, $t_s=1/f_s$ was essentially constant; this factor does not contribute much to waiting time jitter unlike the case in Subsection 6.4.2. Since the slope= f_o is being increased, it appears that this would increase the waiting time jitter. But, as f_o increases, there is a tendency to fall within an earlier stuffing slot since the threshold value for stuffing is achieved sooner. The waiting time jitter period becomes shorter which implies higher fundamental and harmonic frequencies. The net result is the waiting time jitter can be filtered better by the incumbent filter.

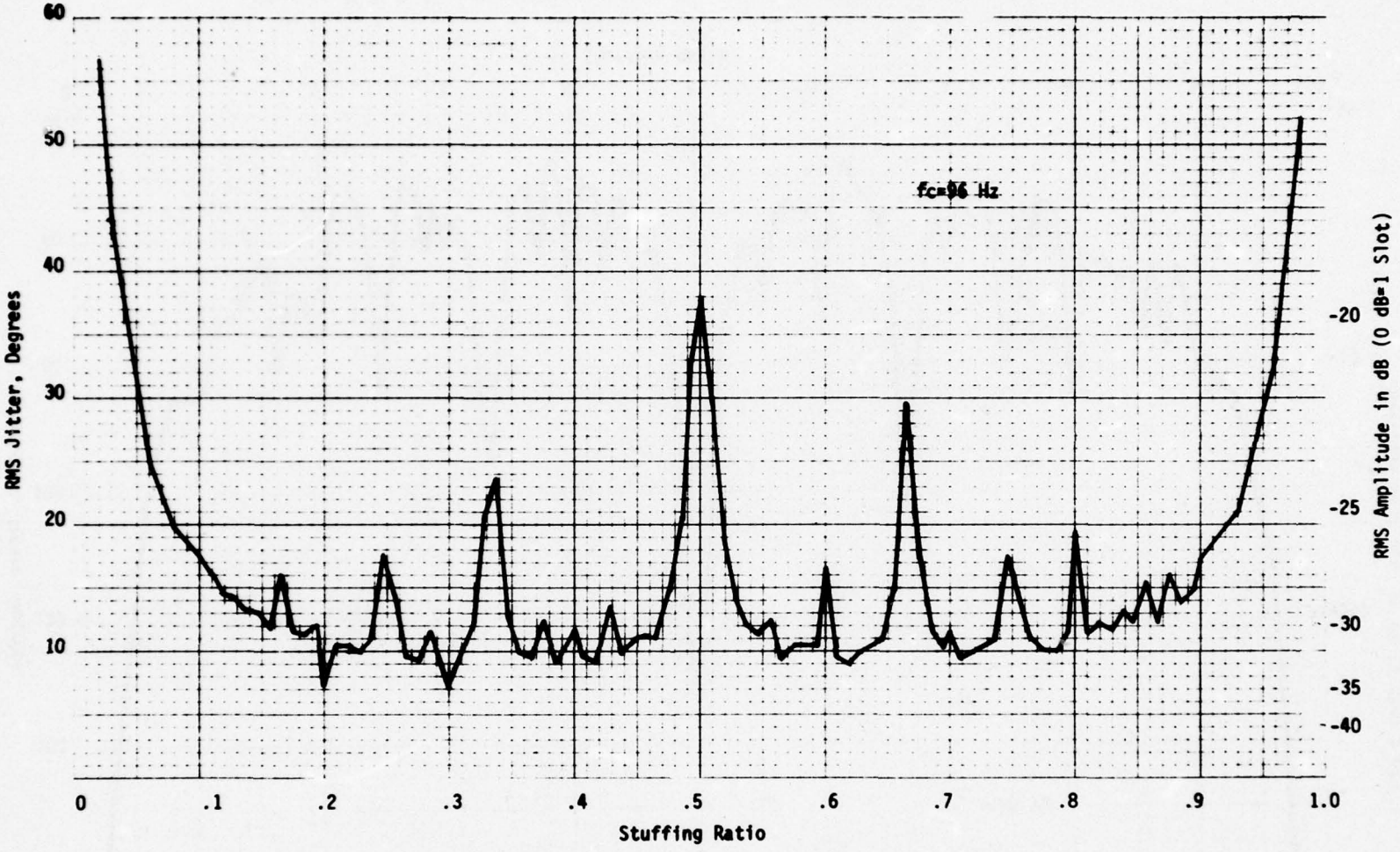


Figure 6.4.6-1. RMS Jitter Versus Stuffing Ratio (ρ) for the Bell M12 for Test 11 in the Test Matrix

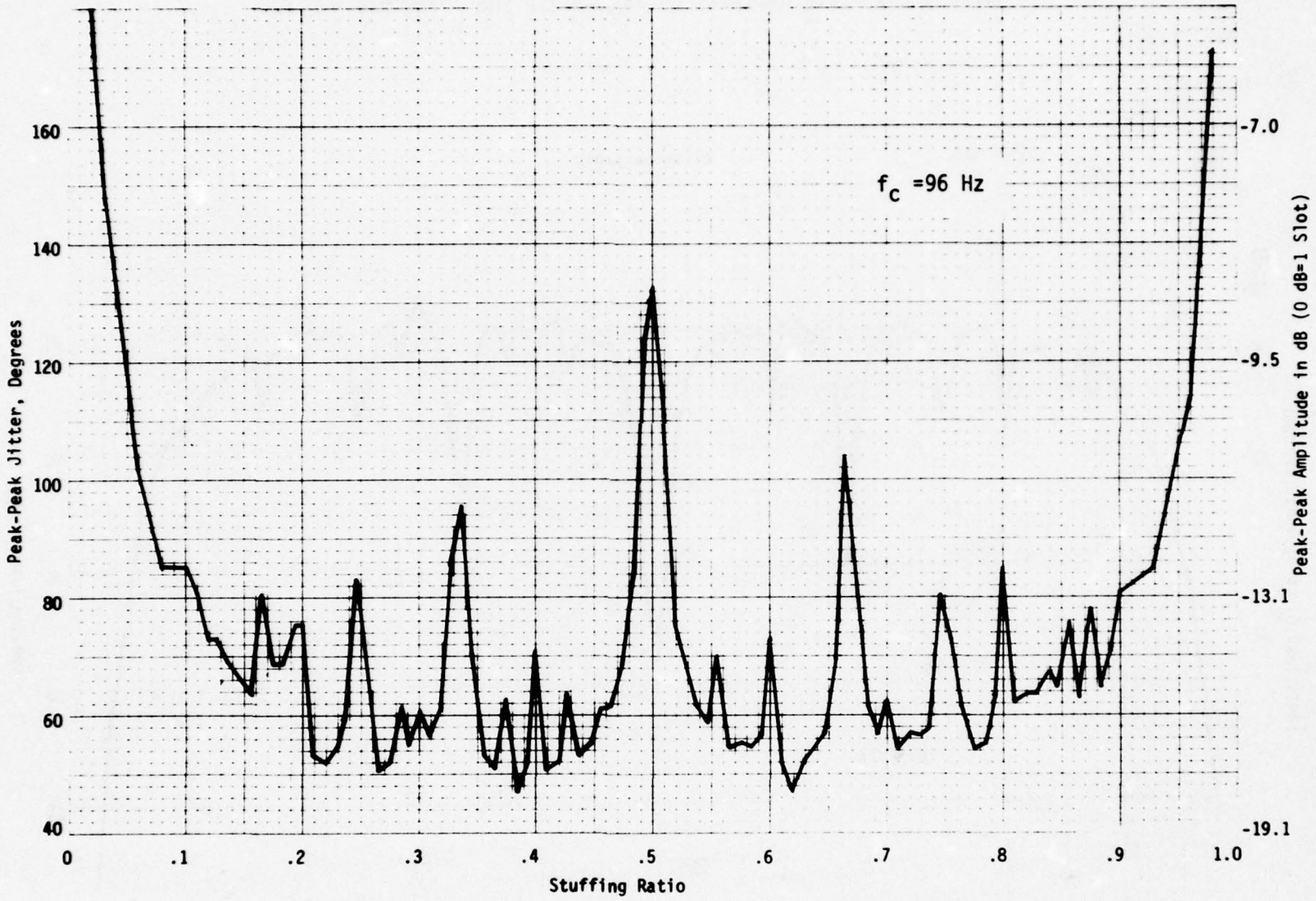


Figure 6.4.6-2. Peak-Peak Jitter Versus Stuffing Ratio (ρ) for the Bell M12 for Test 11 in the Test Matrix

6.4.7 Effects on Jitter When Varying the Tributary Input Channel Rate, T1 (Test 12)

The data for this experiment are tabulated in Table C-14. For this test the T1 rate was varied ±200 bps about the nominal input rate, 1.544 Mbps, in 50 bps step increments. The RMS and peak-to-peak jitter were measured.

From previous discussions, varying T1 changes the stuffing ratio. In fact, this was how the stuffing ratio was controlled when the theoretical curve in Figure 5.1.1-1 was obtained. Observing Figure 5.1.1-1 in conjunction with the data in Table C-14, some interesting conclusions can be reached. Going from a stuffing ratio ρ=.336 to ρ=.298 (-200 bps), the jitter should decrease on regressing from the peak. The experimental evidence verified this since the RMS jitter decreased from 27.4^{o} to 9.7^{o}. Next, going from ρ=.336 to ρ=.371 (+200 bps) in Figure 5.1.1-1, the jitter again should decrease. The experimental data in Table C-14 show that the RMS jitter went from 27.4^{o} to 7.1^{o}. Also, note that Figure 5.1.1-1 implies that ρ=.371 should produce less jitter than ρ=.298. Indeed, from the above discussion, this occurred experimentally.

6.4.8 Effects of Jitter on the HN-74 E-CDS Receive Unit (Test 13)

Test 13 in the test matrix was set up to measure the effects of jitter on the HN-74 E-CDS Receive Unit by varying bandwidth for the Bell M12 and VICOM T1-4000 parameters. A jittered clock from the second level multiplexer/demultiplexer testbed was used to clock an HP-3760/3761 error rate measuring system. First, a smoothed jittered clock from the testbed was input to the HP-3760 Data Generator. Out of the HP-3760 was a pseudorandom binary sequence of 32 bits in length of NRZ data. This sequence was input to the E-CDS Receive Unit. The output of the E-CDS Receive Unit constitutes data plus clock and was checked by the HP-3761 Error Detector. This error detector has been specifically designed for operation with pseudorandom sequences produced by the HP-3760 Data Generator

For this experiment the bandwidth was varied for the Bell M12 and VICOM T1-4000 parameters to observe the bit error rate and the total error count. The bit error rate was the average for a block of 10^{6} bits.

From the data in Table C-15, it is observed that a bit slip was not generated until bandwidths of 1528 Hz for the Bell M12 and 764 Hz for the VICOM T1-4000 were attained. Stepping back to the previous bandwidths of 764 Hz and 382 Hz for the Bell M12 and VICOM T1-4000, respectively, and utilizing the data

in Tables C-2 and C-4 in Appendix C, it is seen that a peak-to-peak jitter of at least 203^{o} for the Bell M12 and 215^{o} for the T1-4000 have to be attained before a bit slip occurs.

It is interesting to note that for bandwidths of 1528 Hz for the Bell M12 and 764 Hz for the VICOM T1-4000, these correspond to peak-to-peak jitters of 279^{o} and 293.1^{o}, respectively. Furthermore, at 279^{o} the bit error rate is 1.3×10^{-4} and at 293.1^{o} the bit error rate is 7.6×10^{-3}, which is larger. The total error counts are 136 for Bell M12 and 7565 for VICOM T1-4000. These results are to be expected since a larger peak-to-peak jitter should produce more errors.

6.5 Examples of the SLMS Smoothing Loop Jittered Outputs

In this subsection examples are provided of the smoothing loop outputs of the jitter simulator shown in Figure 6.3-3. The output of a smoothing loop was displayed on the oscilloscope after being passed through a phase detector as depicted in Figure 6.3-1. A polaroid camera triggered off the oscilloscope was used to obtain the figures in this subsection. These figures are used to demonstrate jitter measurement procedures.

Before discussing the jittered phase outputs, it is worthwhile to observe the driving function. The driving function is the phase difference between the tributary channel clock (T1=1.544 Mbps) and the data transport clock (T1S= 1.545800 Mbps). Figure 6.5-1 illustrates the driving function. This is the same function that was modeled in the software simulation. The waveform in Figure 6.5-1 was obtained using the special phase detector test fixture employed in this study to look at jittered waveforms, measure peak-to-peak phase jitter, and determine slewing rate.

A theoretical example of the jittered phase output for a stuffing interval from a first order smoothing filter is provided in Figure 5.1.2-3. Note how the loop changes character with a change in bandwidth. These types of stuffing intervals existed in the MUXJIT software simulation. Figure 6.5-2 is a typical stuffing interval taken from the smoothing loop output of the hardware simulator after passing through the phase detector test fixture. Note that an apex represents a stuffed pulse. In general, between apexes several stuffing opportunities can occur depending upon the stuffing ratio. The analysis in Subsection 5.1.1 is useful in determining how many stuffing opportunity periods exist and, hence, what is the bit count between apexes. Another way of determining the

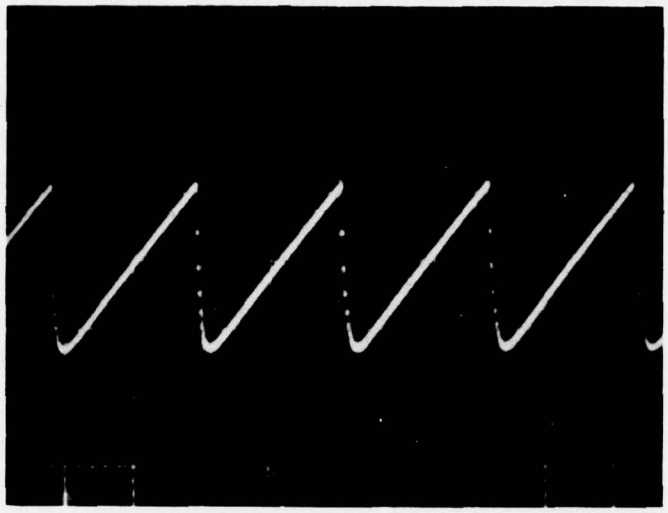


Figure 6.5-1. Input Driving Function, Δ Phase Between T1 and T1S.

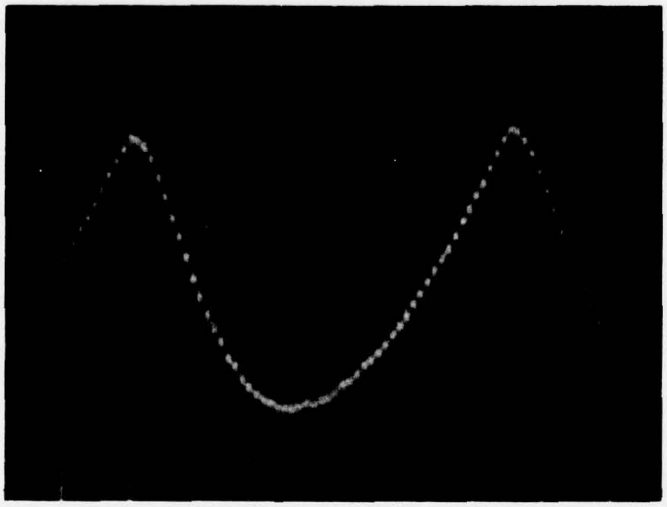


Figure 6.5-2. Example of a Single Stuffing Interval

bit count is to employ the relationship occurring for the distance between apexes, which is obtained from the scope and time base scale factor, and the average tributary data rate.

Going to Figure 6.5-3, where the parameters employed were a 96 Hz bandwidth, 288 bits per stuffing opportunity period, T1=1.544 Mbps and T1S=1.5458 Mbps, here one can observe the phase jitter buildup and reset. The scales are 23.64 degrees/centimeter for the vertical scale and 5 milliseconds/centimeter for the horizontal scale.

The major slew rate occurs during the rapid reset. Note that during rapid reset, as the curve rapidly decreases in amplitude, stuffing opportunities occur and pulses are stuffed. It takes approximately 5½ stuffing periods before completion of reset. For a stuffing ratio of .335, this is approximately 11 stuffing opportunity periods. There are two stuffing opportunity periods per stuffing period for this example. The slew rate can be empirically measured by taking the amplitude difference from the apex of the curve at the stuffing opportunity at the beginning of reset to the end of the reset action (peak at bottom of rapidly resetting portion of the curve) and dividing by the elapsed time measured from a calibrated oscilloscope.

The waveform in Figure 6.5-4 is the same as that in Figure 6.5-3 except for a change in vertical scale factor to 47.28 degrees/centimeter. Later in the discussion waveforms obtained employing wideband filters are presented with this same vertical scale factor. The time base scale factor for Figures 6.5-3 and 6.5-4 was 5 milliseconds/centimeter.

An example of a jittered waveform out of a wideband filter is provided in Figure 6.5-5. The bandwidth 764 Hz and ρ=.315 were used. The vertical scale is 47.28 degrees/centimeter and the horizontal scale is 1 millisecond/centimeter. Comparing these scale factors with the previous example, this represents a much faster slewing condition. It is interesting to note for this case that after reset takes place there is a gradual settlement. The most detrimental slew rate occurs during jitter buildup in a time period which is approximately 2/3 the period between pulse stuffs and is a positive slew rate. The theoretical equations for peak-to-peak jitter, Δy_{p-p}, and the time associated with rapid reset are given in Subsection 5.1.2. These equations pertain to the wide bandwidth case where the slew rate is a problem for the subsequent bit synchronizer in the tandem network. The assumptions behind the equations are not valid for the

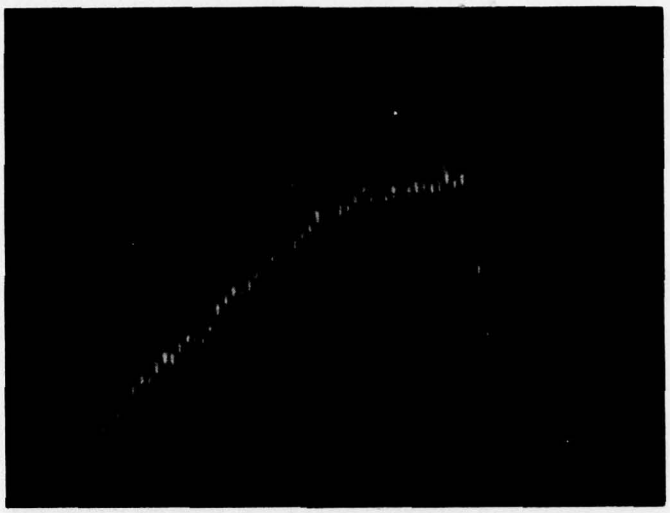


Figure 6.5-3. Jittered Waveform with Rapid Reset for Bell M12 Parameters, f_c=96 Hz, Amplitude Scale of 23.64 Degrees/ Centimeter, and Time Scale of 5 Milliseconds/Centimeter

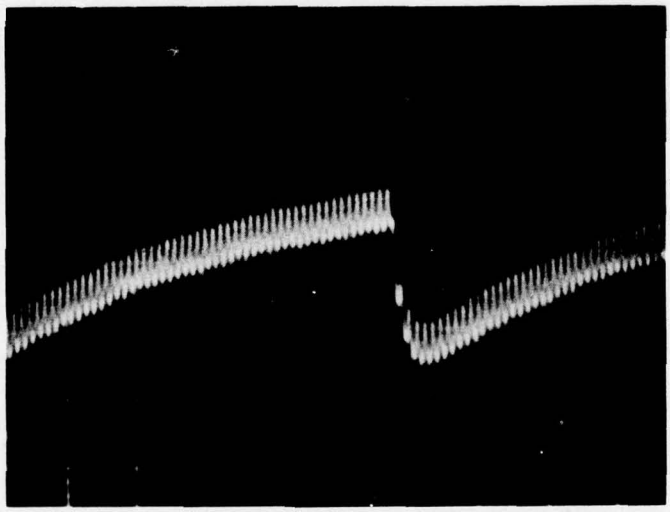


Figure 6.5-4. Jittered Waveform for Bell M12 Parameters, f_c=96 Hz, Amplitude Scale of 47.28 Degrees/Centimeter, and Time Scale of 5 Milliseconds/Centimeter

narrowband case represented by Figure 6.5-3. These equations are useful for theoretically calculating the slew rate ($\Delta y_{p-p}/\Delta t$) as for the case in Figure 6.5-5.

Figure 6.5-6 is the same example as in Figure 6.5-5 with the time base scale factor five times as large. This contracted scale provides a better view of waiting time jitter.

Figures 6.5-7 and 6.5-8 are examples of very rapid slew rates. Figure 6.5-7 represents VICOM T1-4000 parameters and a smoothing loop bandwidth of 382 Hz. Figure 6.5-8 has the same conditions only for f_c=764 Hz. These waveforms are examples of gradual jitter buildup and rapid reset. During rapid reset, the slewing rate becomes detrimental for f_c=764 Hz and causes bit slips in the E-CDS Receive Unit. The scales are 47.28 degrees/centimeter and 1 millisecond/centimeter. Employing these scale factors and measuring Δy_{p-p} and Δt from the figures, the slew rate is .1029 degrees/data unit length for f_c=382 Hz and .1586 degrees/data unit length for f_c=764 Hz. A conversion factor of 1544000 data unit lengths/second was employed to arrive at these numbers.

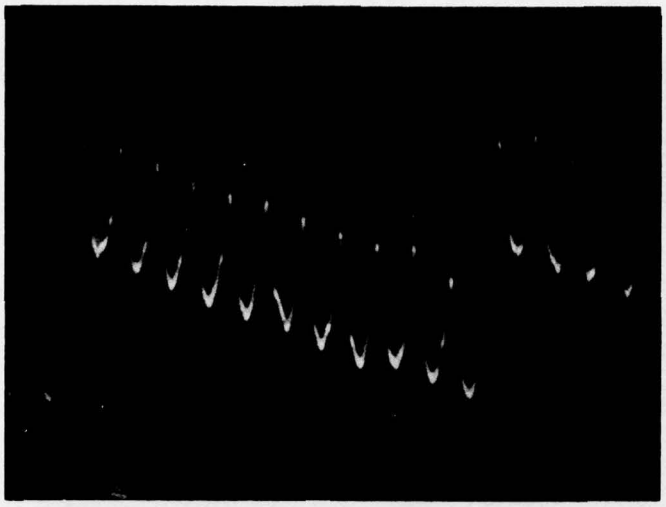


Figure 6.5-5. Jittered Waveform with Gradual Reset for ρ=.315, f_c=764 Hz, Amplitude Scale of 47.28 Degrees/ Centimeter and Time Scale of 1 Millisecond/Centimeter

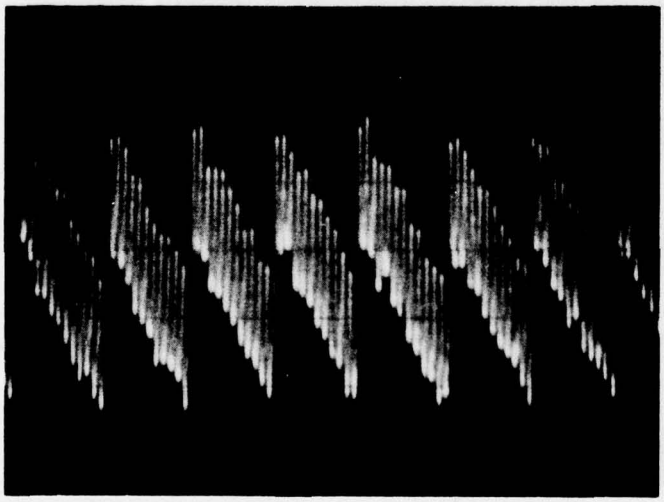


Figure 6.5-6. Jitter Waveform Example of Figure 6.5-5 with a Time Base Scale Factor of 5 Milliseconds/Centimeter

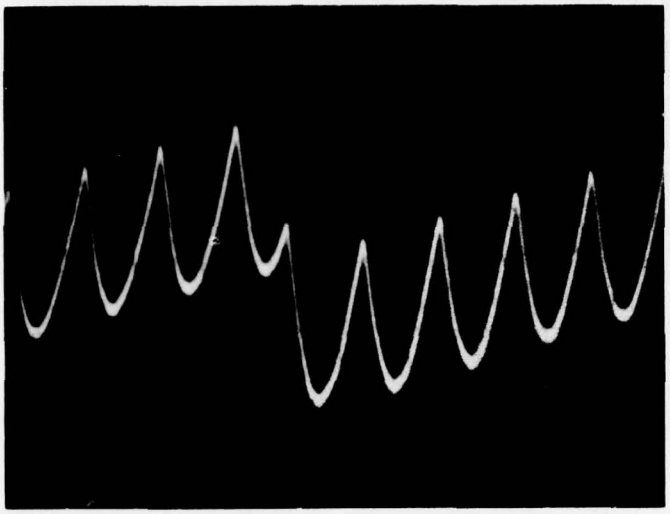


Figure 6.5-7. Jittered Waveform with Rapid Reset for VICOM T1-4000 Parameters, f_c=382 Hz, Amplitude Scale of 47.28 Degrees/Centimeter and Time Scale of 1 Millisecond/Centimeter

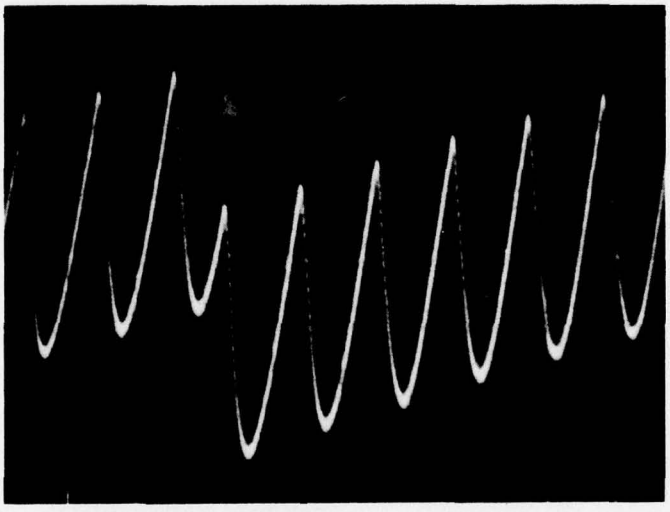


Figure 6.5-8. Jittered Waveform with Rapid Reset for VICOM T1-4000 Parameters, f_c=764 Hz, Amplitude Scale of 47.28 Degrees/ Centimeter and Time Scale of 1 Millisecond/Centimeter

SECTION 7.0

CONCLUSIONS AND RECOMMENDATIONS

7.0 CONCLUSIONS AND RECOMMENDATIONS

This report has covered the results of all four study tasks: 1) jitter analysis, 2) specification development, 3) breadboard testbed development and 4) breadboard test and evaluation. The main thrust of this report was toward providing a record of the analysis investigation, the outcome of the jitter specification development and the results of in-plant testing and evaluation of the breadboard. The breadboard testbed development was covered in the Design Plan for a Pulse Stuffing TDM Network Simulator, a companion document. The interrelationship between the testbed design and the other study tasks is covered in this report.

Basically nine distinct conclusions emerged from this effort.

1) The literature survey (Ref. 2) showed that the impact of cascading N nodes on the RMS output jitter is no greater than $\sqrt{N/6}$ and that the rate of jitter accumulation was no faster than $\sqrt{N}$. The analysis, employing the MUXJIT software simulation, showed that due to the controls built into the pulse stuffing multiplexer mechanism the jitter actually does not appear to progressively increase with the number of nodes, at least for the cases verified. This analysis included reasonably large filter bandwidths. These analytical results are documented in Subsection 5.1.3, Effects of Cascading Second Level Multiplexers. In particular, Figure 5.1.3-1 and Figure 5.1.3-2 are the software simulation results for the VICOM T1-4000 and Bell M12, respectively, which were the cases examined in the analysis. It is observed that when the startup, or transient, effect of the computer program runs were eliminated there was no accumulation of jitter.

   During the test and evaluation phase of this study, experiments were performed on the jitter simulator hardware testbed. The results of these experiments are provided in Subsection 6.4.4, Effects on Jitter for Tandem Configurations (Tests 6, 7, 8 and 9). Observing Figure 6.4.4-1 and Figure 6.4.4-3 for the Bell M12 and VICOM TI-4000, respectively, there was no indication of an increase in jitter when cascading nodes.

   All the experiments discussed in the above paragraphs held all parameters constant except for number of nodes.

2) When running cascaded node experiments, it is necessary to either provide tight controls on other variables which can influence the results or invoke statistical testing techniques to avoid systematic errors. Variations in other

factors such as data transport rates, bits per opportunity, tributary input channel rates, etc., which can influence the amount of jitter, must be either controlled or neutralized statistically so that the impact of cascading nodes is not masked by these variables. As mentioned above all the experiments in this study concerned with jitter accumulation held all parameters constant except for number of nodes. To obtain a feel for the complications that can occur when a parameter is not held constant from node to node, the reader is referred to the results in Subsections 4.1.1, 6.4.1, 6.4.2, 6.4.6, and 6.4.7. It is noted that a variation in bandwidth or a stuffing ratio component will cause a change in peak-to-peak and RMS jitter. From the figures in those subsections, it is seen that the functional relationship between jitter and the independent variable is complicated. Therefore, it is difficult to extract the accumulated jitter effects if the variable(s) is not held constant for a multinode experiment.

3) From this study it was concluded that peak-to-peak phase jitter is more important than RMS phase jitter in determining when a bit slip in a first level multiplexer will occur. Although an RMS value is indicative of the jitter phenomenon, it is peak-to-peak value that prompts the device to fail. The definition of peak-to-peak value had to be clarified during this study. Explicit examples of peak-to-peak values are given in Subsection 6.5. In particular, Figure 6.5-3 is a good example where the jittered waveform has a gradual buildup to a maximum peak value and rapid reset to a minimum peak value. Figure 6.5-8 is an example of a peak-to-peak value which caused a bit slip in the HN-74 E-CDS Receive Unit. The reader is referred to Subsection 6.4.8, Effects of Jitter on the HN-74 E-CDS Receive Unit, where the experiment is fully discussed.

4) Positive (or negative) stuffing methods, which provide the freedom of selecting a data transport rate, permit selection of a stuffing ratio range so that stuffing jitter can be held to an average minimum across the range. This is obvious from Figure 6.4.6-1. The tendency would be to avoid the peaks and to operate in the valleys. The significance of doing this is that jitter filtering can be accomplished with less stringent filtering requirements by avoiding those regions of low frequency and large phase jitter. On the other hand, positive-zero-negative stuffing is affected since it is required to operate across the zero Hz region. This is the ρ=0 region in Figure 6.4.6-1. Here the RMS (or peak-to-peak) value of jitter becomes very large and, in addition, filtering design technology is taxed. Positive-negative stuffing was recommended by the CCITT

Special Study Group D (Ref. 4) to overcome this problem. The concept of positive-negative stuffing is defined in Subsection 3.1, Categories of Pulse Stuffing Multiplexers. The objective of this technique is to introduce higher frequency jitter components which can be filtered out with an economical filter design.

5) Selection of lower stuffing ratios does generate an overall lower waiting time jitter. This can be seen from Figure 4.1.1-3 and the equations on the subsequent page for waiting time jitter magnitude. The waiting time jitter magnitude is equal to ρ bits. It is assumed here that ρ is being controlled by its numerator, the stuffing rate, f_0. The tradeoff to go to a lower stuffing ratio is influenced by the smoothing loop complexity required to remove the low frequency pulse stuffing jitter components which are the major contributors to jitter for low stuffing ratios.

6) For a fixed smoothing loop bandwidth, there are distinct differences in the amount of jitter that can arise depending upon how the stuffing ratio is controlled. For a particular value of stuffing ratio, a different peak-to-peak or RMS value of jitter can occur if the stuffing ratio is controlled by a different parameter. For example, if the data transport rate is used to obtain a particular stuffing ratio, the jitter will, in general, not be the same as obtaining the same stuffing ratio by varying the bits per opportunity in the control channel. These points can be illustrated by comparing Figure 6.4.2-1 (varying stuffing ratio by manipulating BPO) with Figure 6.4.2-1 (varying stuffing ratio by manipulating the data transport rate) on a point by point basis. The bandwidth was fixed at f_c=96 Hz for both graphs.

7) Tradeoffs between first order and second order smoothing loops are swayed by economics towards a first order loop. As discussed in Subsection 4.1.5 and illustrated in Figure 4.1.5-1, the second order loop provides no additional filtering and, in fact, has the added complication of enhancing jitter over a certain band of frequencies (note the case for ζ=0.3 in the graph). However, a narrow bandwidth first order loop requires a larger phase error to generate a frequency deviation in the VCO (Ref. 11). To accommodate the larger phase errors, it is necessary to use an extended phase detector. Practical limits in resolving phase errors accurately in extended phase detectors determine the narrow bandwidth limits on a first order loop. On the other hand, there are practical limitations in acquiring a signal with an extremely narrow bandwidth.

8) Because of tracking requirements second order phase locked loops are employed for bit synchronizer applications. Bandwidth requirements for bit synchronizers are selected in a tradeoff between narrow bandwidths stemming from noise and large bandwidth arising from tracking considerations for jittered

inputs (Ref. 1, 3, 15). This trade-off can be done on a basis of signal-to-noise impact on signal acquisition. In Section 5.2, Input Jitter Characteristics of First Level Multiplexers, experiments were discussed, where VICOM parameters were used, which studied the effect of second order bit synchronizer bandwidths on pulse stuffing jitter. It can be seen from Figure 5.2-3 that increasing the bit synchronizer bandwidth produces a reduction in peak error. The definition of peak error is the peak error at the phase detector output in the phased locked loop and corresponds to θ_e in Figure 4.1.3.

The model in Section 4.1.3 would have to be extended to study the effects of noise on peak error. This model could be incorporated in MUXJIT. Then the appropriate tradeoffs between narrow bandwidth requirements stemming from noise bandwidth limitations and large bandwidth requirements arising from tracking considerations could be evaluated.

9) The HN-74 bit synchronizer in Figure 3.4-1 is stable over a wide range of demultiplexer smoothing loop bandwidths with respect to being susceptible to a bit slip. From the data tabulated in Table C-15 and discussed in 6.4.8, the jitter must be well over 50% of the data unit interval with a slew rate in excess of .1 degrees/data unit interval. A discussion of the definition of slew rate is provided in Section 6.5. An example of calculating the slew rate is given at the end of Section 6.5. This is for the VICOM T1-4000 case. Employing an oscilloscope trace captured on polaroid film, the Bell M12 case was calculated in a similar manner. For both cases the slew rate was in excess of .1 degrees/data unit interval before a bit slip occurred.

The recommendations that have emerged at this time call for an extension of the analytical and testbed investigation in five given areas. Such recommendations are considered necessary in view of the additional questions that have surfaced during this study. It is felt that the study effort could be easily extended through these five areas in light of the analytical and hardware tools developed and information already generated. These suggested tasks are recommended as natural extensions of this study since they would complement the present study with increased depth.

1) Extension of analytical investigation by modifying MUXJIT to include the positive-negative stuffing approach recommended by the CCITT Special Study Group D. This stuffing approach according to the recommendation provides stuffing frequency offsets which can be more easily removed by the smoothing loop. This would avoid the low frequency stuffing jitter problems of the now more conventional positive-zero-negative approach. This effort should be enhanced by also including a paper analysis.

2) As an extension to the analysis task for establishing phase jitter tolerance limits for a first level multiplexer it will be necessary to exercise MUXJIT using a second order smoothing loop employing the tolerance acceptability criteria established as a result of the investigation using the second level multiplexer testbed and the HN-74 E-CDS receive circuitry. The breadboard testbed Test and Evaluation Phase should provide the insight to formulate an investigation and establishment of criteria for phase jitter tolerance as well as evolving a more sophisticated understanding of design requirements for a bit synchronizer in a first level multiplexer.

3) The waiting-time jitter smoothing loop criteria developed should be investigated for a more complete understanding of its relationship to stuffing ratios which yield short sequence periods. The heuristic approach undertaken was primarily intended to capitalize on the results of MUXJIT. It is felt that a more detailed study should be undertaken to solidify the interpretation of these results.

4) An extension of the hardware testbed data collection and analysis of jitter by varying the stuffing ratio for various bandwidths would elicit insight to the characteristics of jitter with respect to a particular stuffing ratio parameter variation and bandwidth. Curves were derived for a single bandwidth while controlling the stuffing ratio. This task would expand that analysis by obtaining additional curves. Therefore, a more complete characterization of jitter could be attained.

5) Another test and evaluation effort which would accrue benefits would be to generate curves of slewing rate as a function of bandwidth and stuffing ratio. The slewing rate could be measured by the techniques described in Subsection 6.5. This would provide a more complete characterization of slewing rate with respect to bandwidth and stuffing parameters.

As part of a long term enhancement to the results of the present study, it is suggested that the following areas would yield fruitful results:

1) Development of a second order smoothing loop to investigate the practical limitations of narrow bandwidth loops in light of the VCO frequency offset requirement invoked by tributary input channel tolerances. Conduct a testing program to verify analytical results derived while establishing second order loop design requirements.

2) Expand MUXJIT to include an analysis of the pulse slicing techniques used by digital smoothing loops and, hence, provide insight into this phenomena.

3) Modify MUXJIT to include the capability to simulate the non-isochronous stuffing intervals generated by schemes such as a reversed binary count sequence for establishing port stuffing opportunities. This would permit more accurate simulation of the AN/GSC-24. Also, modeling of coarse rate correction schemes should be considered.

4) Expand the design and test effort to provide a definition and specification for development of a Jitter Measurement Test Set which will be used as a criteria for testing prototype and fielded Pulse Stuffing Second Level Multiplexers. From efforts to date it is apparent that specifically defined equipment and test procedures would greatly enhance the specification capability and diminish the measurement problems.

5) Develop a bit synchronizer simulator circuit, with a second order tracking loop, which can be implemented into the testbed. This would allow investigation of jitter effects on bit synchronizers in terms of tracking loop filter design parameters. Phase error could be measured for various jitter inputs and tracking loop parameters. This would provide more empirical data on the interaction between second level multiplexers and bit sync circuits.

The latter recommendations are considered longer term than the initial five recommendations, which are of immediate consideration.

APPENDIX A
RECOMMENDED JITTER SPECIFICATIONS

1.0 INTRODUCTION

From the Analysis Task of this study, specifications have been identified which are candidates for specifying jitter in pulse stuffing TDM networks. It is assumed that first and second level multiplexer/demultiplexer units can be considered somewhere between a Type B1 prime item procurement and Type B2 critical item procurement, possibly leaning toward the prime item category as defined in MIL-STD-490, Military Standard Specification Practices. In a specification for a multiplexer/demultiplexer, these specifications would be incorporated in paragraph 3.2 Characteristics and paragraph 4.2 Quality Conformance Inspections. Paragraph 3.2 is part of 3.0 Requirements, and paragraph 4.2 occurs under 4.0 Quality Assurance. To delineate it further in accordance with MIL-STD-490, these specifications would appear in subparagraph 3.2.1 Performance. Presently, many of the multiplexer/demultiplexer specifications do not delineate it to this degree and place comparable specifications of this type in a convenient subparagraph of paragraph 3.2, which is then entitled Performance Characteristics.

A systems approach has been utilized to define the jitter specification candidates in this report. Since the specifications are to be independent of a particular system, a thorough literature search and extensive computer simulation runs were performed to determine similar characteristics of multiplexers/demultiplexers which could be incorporated in a specification. Furthermore, the issue involved is a digital interfacing problem.

Therefore, the intrinsic characteristics of the inputs and outputs must be utilized in a performance specification. Considering the inputs and outputs of a system as a set of time functions, the restrictions and measures must apply to the domains and ranges of these functions. This aids in divorcing the specifications from a particular design, which is important in systems that contain first level and second level multiplexer/demultiplexer nodes developed independently of each other.

In choosing a set of candidate specifications, the first level demultiplexer was considered first. It was considered first since its inputs limit the variation in range of the second level demultiplexer output. The output of the first level demultiplexer is not considered. The analysis of voice distortion was beyond the scope of this study. Through the efforts of this study, the limitations on the outputs of the second level demultiplexer have been identified as the following:

A. The maximum peak to peak jitter that should occur at the output of the device.

B. Tandeming specification for jitter at the output of the n^{th} node of second level multiplexer/demultiplexer pairs in tandem.

C. Maximum slew rate that should occur at the output of the device.

D. The input static frequency range $f_1 \leq f_o \leq f_2$ about the nominal frequency, f_o, that the device can tolerate.

Since the input to a second level multiplexer has the possibility of being an output of a second level demultiplexer, and the entities being measured must be compatible for specification purposes, items A thru D can be used to specify the digital input to the second level multiplexer.

In Section 2.0 of this Appendix, each jitter specification is described in more detail. Methods for measuring the characteristics are also described.

2.0 DISCUSSION OF JITTER SPECIFICATIONS

2.1 Maximum Output Jitter Specification

Specification:

The peak to peak jitter on the output data and timing signals shall not exceed 33 percent of the nominal data unit interval.

Discussion:

The above specification is similar to the output jitter specification that appears in many of the device specifications. As has been pointed out in this report, peak to peak is more meaningful than RMS. At times it might be easier to measure the RMS value and then calculate the peak to peak value

assuming that peak to peak values are well behaved and can be related to RMS values. The purpose of this specification is to introduce which "jitter" is to be measured. The reader is referred back to Subsection 6.5 for examples of peak-to-peak phase jitter. By peak-to-peak phase jitter is meant the change in amplitude between the peak that occurs at a stuffing opportunity reset and the minimum peak that occurs after rapid reset as in Figure 6.5-3 or gradual reset as in Figure 6.5-5. A discussion as to the number of bits that occurs between peak-to-peak points for rapid buildup or rapid reset was provided in Subsection 5.1.1 and explained further in Subsection 6.5. The argument depended upon whether m or m+1 stuffing opportunity periods occurred within a stuffing period. The question can be resolved with the argument and examples given in Subsection 5.1.1. In the quality assurance paragraphs of the specification, measurments are left to the discretion of the manufacturers. A technique is given below for measuring jitter. This technique must also be employed in a specification for tandeming of second level multiplexer/demultiplexer pairs.

2.1.1 Measurement for a Maximum Output Jitter Specification

Measurement:

Take the jittered clock from the demultiplexer smoothing loop output and compare it with a nominal stable reference source frequency input into the network. This comparison should be done in a phase detector. The phase detector should make this measurement by integrating between the positive edge of the stable reference signal and the positive edge of the smoothed jittered

signal from the demultiplexer. The integrated value is sent to a sample and hold circuit. The output of the sample and hold circuit is displayed on a calibrated oscilloscope to provide a display of the phase variation of the jittered waveform. The peak-to-peak value can be obtained by observing the waveform with a polaroid snapshot or directly from the scope. The peak-to-peak value is defined as the difference between the maximum and minimum amplitude excursions that occur.

Discussion:

A special phase detector test fixture was developed for this program and implemented into the test configuration as pictured in Figure 6.3.1-1. Examples of smoothed jitter outputs as measured by the test fixture are given by Figures 6.5-2 through 6.5-8 in Subsection 6.5. Peak-to-peak values can be measured off the scope as discussed in Subsection 2.1 of this Appendix. Furthermore, to obtain RMS values for the test and evaluation phase of this study an RMS meter was attached to the output of the phase detector test fixture.

There are other measurement techniques such as using a dual trace scope with an input calibration signal and a jittered waveform. This method is frequently used. However, it is difficult to read the RMS and peak-to-peak value off the face of the scope. The method described above provides peak-to-peak and RMS values.

2.2 Second Level Multiplexer/Demultiplexer Tandeming Specification

Specification:

With a stable input data rate, within the tolerance range specified herein this device specification, as an input to the first multiplexer/demultiplexer pair (node), the peak-to-peak jitter output of the n^{th} node shall not exceed that which is specified in the Combined Effects of Jitter Specification as input to the $(n + 1)^{th}$ node.

Discussion:

During the analysis phase of this study, it was noted from the simulations that the peak-to-peak jitter versus number of nodes had a small positive slope. This is due to initialization and transient effects in the simulation. Jitter accumulation appears to be negligible. However, if an upper bound is desired, the following addition can be made to the specification:

> "Furthermore, the jitter between the n^{th} and $(n + 1)^{th}$ node shall accumulate at a rate not to exceed the tandem factor, G_T, which is the rate or change of jitter between two nodes in tandem. G_T shall have units of peak-to-peak jitter/data unit interval. The relationship between the number of allowable nodes in the network, G_T, and the maximum allowable jitter, J_{max}, input to a node is found in the Combined Effects of Jitter specification and is $G_T N \leq J_{max}$."

Therefore, an upper bound on the slope would be an appropriate specification. This would prevent the jitter from possibly exceeding one of the standard specifications tabulated in Subsection 2.4.

Although not referred to in the tandem specification, specifications for bit count integrity, slewing specification, phasing, ringing, etc., must still be maintained. It is tacit that these specifications not be violated for either the multiplexer or demultiplexer in a node and for each node in the network.

2.2.1 Measurement of the Tandeming Specification

The Peak to Peak jitter should be measured at each node. A straight line is fitted to the data and the slope, G_T, is obtained. This value should be normalized to the expected data unit length.

2.3 Maximum Slew Rate Specification

Specification:

Each output port (single or strapped) shall contain provisions to smooth the effect of destuff actions. The maximum variation in phase difference between the output port data and timing signals and a stable phase reference signal at the multiplexer port timing input shall not exceed a change in peak-to-peak phase jitter of Δy_{p-p} radians over a time period, Δt seconds, or less. Bit-to-bit phase variation shall not exceed the jitter requirements of the Output Jitter Specification.

Discussion:

The rationale for this specification is contained in Subsections 5.1.1, 5.1.2, and 6.5 of this report. The maximum phase rate of change, and the time at which there would be the greatest likelihood of a loss of sync, occurs in the vicinity of rapid phase reset or rapid phase buildup as described in Subsection 2.1 of this Appendix and illustrated in Figure 6.5-3 (rapid phase reset) and Figure 6.5-5 (rapid phase buildup). If the slewing rate over a time period is large, the ensuing tracking circuit will have difficulty following it. Both first order and second order filters have difficulty responding to sharp velocity changes. The design equations which imply the form of the above specification and which provide direction for determining values of Δy_{p-p} and Δt and, hence, the slew rate ($\Delta y_{p-p}/\Delta t$) for the spec writer are the following:

$$m < \frac{1}{\rho} < m + 1/2$$

$$\Delta y_{p-p} = \rho(m + 1) + \frac{e^{-2\pi f_c \rho(m+1)}}{1 - e^{-2\pi f_c}} - \frac{1}{2\pi f_c}\left[1 + \ln\frac{2\pi f_c}{1 - e^{-2\pi f_c}}\right]$$

$$\Delta t' = \rho(m + 1) - \frac{1}{2\pi f_c} \ln\left[\frac{2\pi f_c}{1 - e^{-2\pi f_c}}\right].$$

$$\Delta t = \Delta t' T$$

$$m + 1/2 < \frac{1}{\rho} < m + 1$$

$$\Delta y_{p-p} = -\rho m + \frac{2 - e^{-2\pi f_c \rho m}}{1 - e^{-2\pi f_c}} - \frac{1}{2\pi f_c} \ln\left(\frac{2\pi f_c}{1 - e^{-2\pi f_c}}\right)$$

$$\Delta t' = \rho m + \frac{1}{2\pi f_c} \ln\left(\frac{2\pi f_c}{1 - e^{-2\pi f_c}}\right).$$

m - largest integer in $1/\rho$.

T - 1/(Stuffing Rate)

f_c - First order bandwidth cutoff frequency.

ρ - Stuffing ratio

Δy_{p-p} in these equations is the peak-to-peak phase jitter of the single stuffing interval waveform as pictured in Figure 6.5-2 and either the rapid buildup or reset slew rate for a wideband filter as depicted in Figures 6.5-5 and 6.5-7. For measurement purposes Δy_{p-p} also refers to the rapid reset rate illustrated in Figure 6.5-3; however, for this narrowband case the theoretical equations do not hold. Δt is the corresponding time interval between the maximum and minimum amplitude points of the rapid reset or buildup slew rates. Note for the narrowband case as in Figure 6.5-3, there are several stuffing intervals that occur during reset. The derivation for Δt of the above equation is no longer valid. Δt must be measured empirically to determine the slew rate.

Equations for a second order loop are more complex, and program resources did not permit the analysis. The above analysis was prompted by the GASP IV simulation results.

2.3.1 Measurement of the Slewing Rate Specification

This measurement is made using the setup described in Subsection 2.1.1. Observing the figures in Subsection 6.5, the slew rate that is of interest is the rapidly resetting or phase buildup slew rate. Measurement of the peak-to-peak value as discussed in Subsection 2.1.1 and its corresponding Δt should be

used in the slew rate specification. For the wideband case, the equations given in the preceding subsection should be good approximations to the values obtained from an oscilloscope. The value of Δy_{p-p} from Figure 6.5-8, which causes the E-CDS Receive Unit to bit slip, is 269.5 degrees. Δt is 1.1 milliseconds. This results in a slew rate of $.1586^{o}$/Data Unit Interval.

The oscilloscope measurement for Δt can be related to the tributary input channel data rate by the following equation:

Number of Data Unit Intervals = T1 * Δt.

T1 is the tributary data channel rate. The number of stuffing opportunity periods can be related to Δt by

Number of Stuffing Opportunity Periods = Number of Data Unit Intervals/bits per opportunity.

If the data channel rate is changed, Δt must vary in order to keep the number of bits constant.

2.4 Static Data Signal Range Specification

Specification:

The data signal input range that a device should accept is defined by $f_1 \leq f_0 \leq f_2$. f_1 and f_2 are the lower and upper limits, respectively. f_0 represents the data signal range parameter.

Discussion:

This range is a static range; there is minimal slewing between frequencies. Frequencies outside the range are characterized by bit slips occurring on the output of the device or the following conditions are violated:

A. Rise and Fall Time

The rise and fall time, T_r and T_f, respectively, of the digital output signal between the 10% and 90% points shall not be degraded. For NRZ or bipolar outputs, these times are generally given in the standard multiplexer/demultiplexer specification.

B. Ringing (Data and Timing Signal)

The standard ringing specification shall not be exceeded.

C. Phasing

The standard phasing specification shall not be exceeded.

D. Combined Jitter Effects Specification

The combined jitter on the input of the succeeding node shall not be exceeded according to the combined jitter effects specification for that node.

From the literature search and document perusal, it is apparent that the internal circuits cannot tolerate all frequencies. The receiving circuit has a limited bandwidth. It is assumed that each frequency in the range is generated independently; i.e., there is minimal slewing from one frequency to another.

2.4.1 Static Frequency Range Measurement

Measurement:

The input waveform can be generated with a frequency synthesizer. The output of the node can be measured with a frequency counter to determine the bit rate, oscilloscope and polaroid camera to make waveform quality measurements, and a phase detector test fixture for jitter measurements.

APPENDIX B
SOFTWARE SIMULATOR (MUXJIT) DESCRIPTION

Computer Simulation of Timing Jitter Generated by A Network of Cascaded Pulse Stuffing Multiplexer/ Demultiplexer

The purpose of this simulation is to compute the phase (timing) jitter created by cascading a group of pulse-stuffing second level multiplexer (MUX)/ demultiplexer (DEMUX)/ smoothing loop sets. This simulation will address a generic system where information for a specific system can be derived by establishing the operational parameters to be those of the specific system.

Statement of the Problem

The system to be simulated consists of a given number of nodes of what is referred to as a second level multiplexer/ demultiplexer/ smoothing loop (MUX/DEMUX/ SMOOTHING LOOP) set. The best approach to define the problem is to first define the specific hardware and its operation, then from that definition explain the problem.

In order to define the specific hardware it is best to define the modifying description in its name. The adjective second level stems from its location in the system with respect to the transfer of raw data. The first level multiplexer takes 24 voice (or voice equivalent digital data) channels and combines them into a single (Bell T1 Data Channel - 1.544 MHz) data system. The second level multiplexer takes T1 Data Streams and combines them into a higher rate bit stream (i.e. Bell T2 Data Channel - 6.312 MHz or some other equivalent). There are third level multiplexers in the Bell System hierarchy.

The term pulse stuffing defines a system approach for transferring data from a source through a bit stream which is asynchronous to the source. Basically the

transferring bit stream carries n source channels. The segment of the transferring bit stream corresponding to a single source is plesiochronous (almost synchronous) to the source and operates at a rate which is slightly higher than the upper range of the source.

The corresponding segment of the transferring bit stream consists of overhead bits and data bits. There are two distinct approaches to pulse stuffing, positive stuffing and positive-zero-negative stuffing. In the positive stuffing approach, the rate of the transferring data bits exceeds the source data rate. The difference is made up by injecting or stuffing pseudo bits into the steam of data bits. In the basic positive-zero-negative stuffing approach the rate of the transferring data bits is equal to the nominal value of the sources data rate. If the source data rate is below the nominal value the system operates identically to the positive stuffing approach. However, if the source data rate is above the nominal value the difference is compensated by removing bits from the data bit stream and transporting the information in the overhead bits. This latter method is the negative stuffing approach.

To continue the description of the problem it is next necessary to describe the operation of the three hardware modules-multiplexer, demultiplexer, and smoothing loop. The description will be conducted in terms of a single T1 channel since the operations and data transporation of each T1 channel are kept separate from each other. The first operation is described from the operation of the multiplexer input for a given channel. Each input has an individual elastic buffer which has data written into it by the source clock (T1 channel) and the data is read from the buffer by the multiplex output clock (i.e. T2 channel). For the purpose of

this discussion we will refer to the data transport rate of the multiplexer as a T2 rate. It will be pointed out that this T2 rate (different than Bell T2 Channel) varies among the various multiplexer systems being considered. The multiplex input port (i. e. T1 Channel) doesn't vary for the systems being considered here. This T2 rate considers only the transferring data stream data bits. The overhead bits are in excess of this T2 rate. Anyhow, since the elastic buffer has data being written in at one rate (i.e. T2) eventually this operation will lose or gain a bit. At this point it is decided that a pseudo bit must be injected or a bit must be removed to re-align the phase relation of the data streams. Of course to do this manipulation the insertion or removal must be controlled so that the DEMUX knows when to do the inverse operation. This is accomplished by making use of the overhead bits to convey the "stuffing bit" location to the DEMUX. Therefore after the phase relationship is one bit behind or ahead an addition phase delay results from this fact. The delay between the actual stuffing requirement and the overhead bits which must transpire before the actual stuffing is accomplished results in "waiting-time" jitter since the relationship is not fixed.

In the DEMUX the data bits are normally written into an elastic buffer, the only exception being the stuffing bits. When the overhead bits identify a stuffing bit the clock is inhibited and the bit is not written into the buffer. If excess data information were carried in the overhead bits they are written (inserted) into the elastic buffer at the correct location in the bit stream. This abruptly discontinuous clocking of the bit stream is called "stuffing" jitter. We have just briefly described the two elements of jitter associated with a pulse stuffing multiplexer system.

The other hardware module-the smoothing loop-is used to generate the clock that reads the data from the elastic buffer. It is a phaselock loop which attempts to smooth the abrupt discontinuities and other jitter. It is ideally intended to clock out the data stream at a stable T1 rate. The smoothing loop design should allow any long-term variation (T1 slew rate) through to prevent data overflow or underflow at the DEMUX elastic buffer. The only information available to the smoothing loop to determine T1 rate is the jittered output of the DEMUX as it is read into the elastic buffer. These high frequency abrupt disruptions are undesirable elements since they affect the bit synchronizers used in a first level DEMUX to receive the T1 channels output from the second level DEMUX/ Smoothing Loop. Low frequency variation which do not affect the bit synchronizers are permissable. However many of the bit synchronizers presently used have a very narrow bandwidth. Ideally the only slew information which needs to be tracked is that of the original T1 channel input, other slew is noise introducted by the pulse stuffing multiplexer system. The smoothing loop should act as a low pass or highly overdamped jitter which only reacts to low frequency variation (original T1 channel slew rate).

To conclude the statement of the problem it is necessary to briefly describe the effect of cascading second level MUX/DEMUX/Smoothing Loop sets. This can be accomplished by describing the operation of the second hardware set in the cascade, more specifically by describing the operation of the MUX in this set since that is where the impact lies. If we assume that the T1 channel input is no longer a stable source but rather it has clock jitter then the input being written into the MUX elastic buffer is being done with a jittered clock. In essence this

jittered clock varies the rate of loading of the elastic buffer and by doing so it could vary the location of the one-bit out-of-phase decision point from which the "pulse stuffing" decision is being rendered. Since the clock is jittered about the long-term T1 rate and the jitter is significantly reduced by the smoothing loop the variation of the decision point is small. Because the re-adjustment of clock phase is not performed immediately but is rather delayed until the precise location in the T2 channel frame arrives, variation may or may not be noticable during any one given frame, but could be noticeable over several frames. Therefore the effect of cascading could introduce a low frequency component (i.e. simply an aggravation of the "waiting-time" jitter) which the smoothing loop might not filter. This effect could become worse over several cascaded sets.

Because this is a sampled data system with discrete-time inputs it is difficult to formulate an analysis approach, specifically because of the non-periodic discontinuous nature of the discrete-time inputs. It is therefore necessary to use a software simulation to derive analysis answer to the problem of measuring the input of "waiting-time" jitter and the cascading effect.

Model Description

The computer simulation model can be described as an extension to the statement of the problem. In essence to represent each hardware module set (node) two major things are needed:

a) A discrete-event simulation of the periodic phase correction opportunities with a decision criteria of when to make the phase correction.

b) A continuous (either a state equation or a difference equation) simulation of the smoothing loop's operation on the phase relationship of the jittered signal going through the smoothing loop with respect to a stable input signal. In other words since this is a linear system model (all elements are additive) a perturbation model of phase jitter is a prefered approach for computational accuracy.

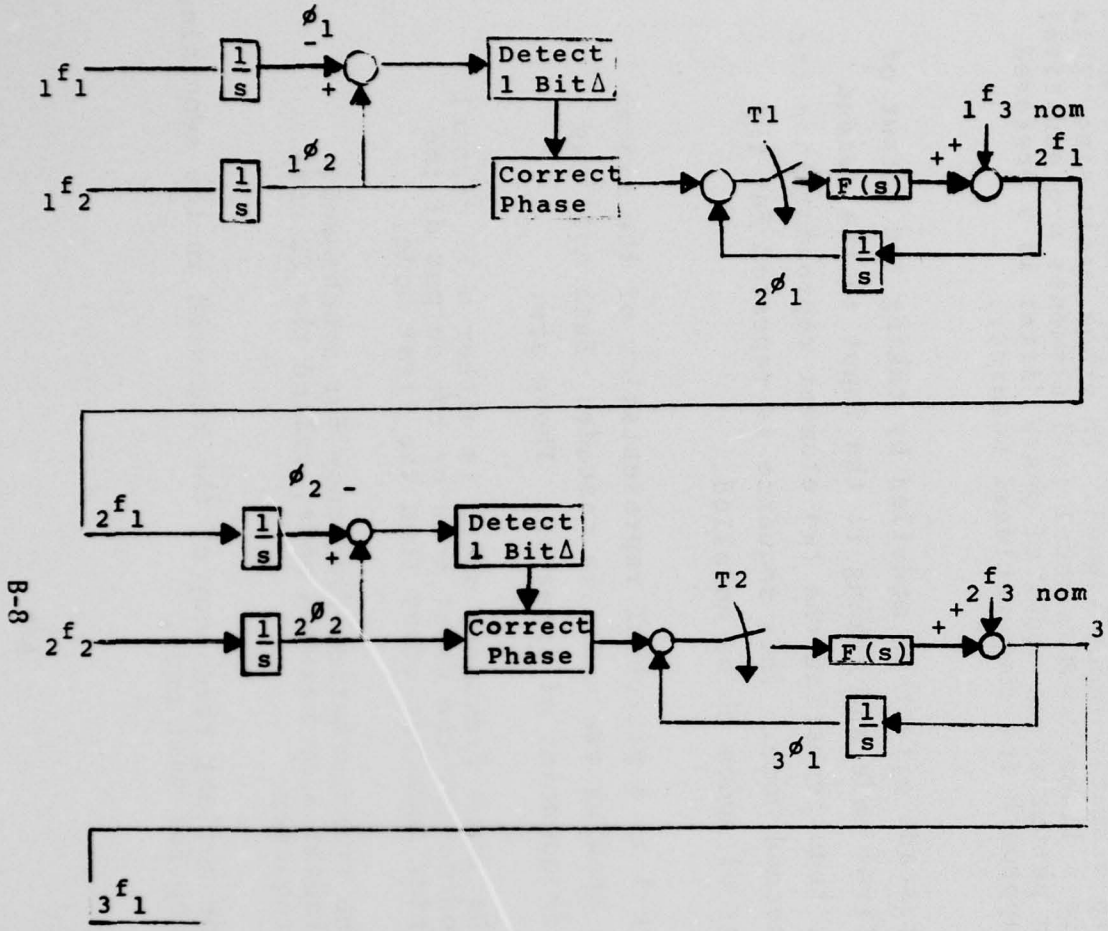
The cascade effect is modelled by taking the output of the first node and making it the input to the second node, then repeating the two element representation for the second node. This sequence is repeated for the number of nodes to be modelled.

Figure 1 is a pictorial representation of the System Model showing two nodes in cascade. Each node has four frequencies of interest. These are:

a. The input frequency which is either a T1 channel source for the first node or the output of the prior node for other than the first node.

b. The transportation frequency for synchronous transmission between node, called the T2 rate frequency.

c. The nominal frequency of the VCO used in the smoothing loop for that node.



$1^{f}1$ = T1 Rate input frequency

$1^{f}2$ = T2 rate frequency/node 1
= $1^{f}1 + \Delta_1 f_2$

$1^{f}3$ = VCO nominal frequency/node 1
= $1^{f}1 + \Delta_1 f_3$

$2^{f}1$ = node 1 output/node 2 input

$2^{f}2$ = T2 rate frequency/node 2
= $1^{f}1 + \Delta_2 f_2$

$2^{f}3$ = VCO nominal frequency/node 2
= $1^{f}1 + \Delta_2 f_3$

FIGURE 1
System Model

d. The output frequency which is the input frequency to the following node.

The phase error sampler in the loop is driven by the T2 rate.

In order to complete the overall model it is necessary to model a bit synchronizer as the final element to these cascaded nodes. The bit synchronizer is a phaselock loop, the difference is that the parameter of the interest for the bit synchronizer is the phase error (the output of the phaselock loop's summing node or the input to the sample).

Figure 2 shows the translation of the system model to the system perturbation model. This perturbation model also shows a two-node cascade. It is derived by setting the T1 rate input frequency equal to zero ($_1f_1=0$). This is the model that will be implemented in the simulation.

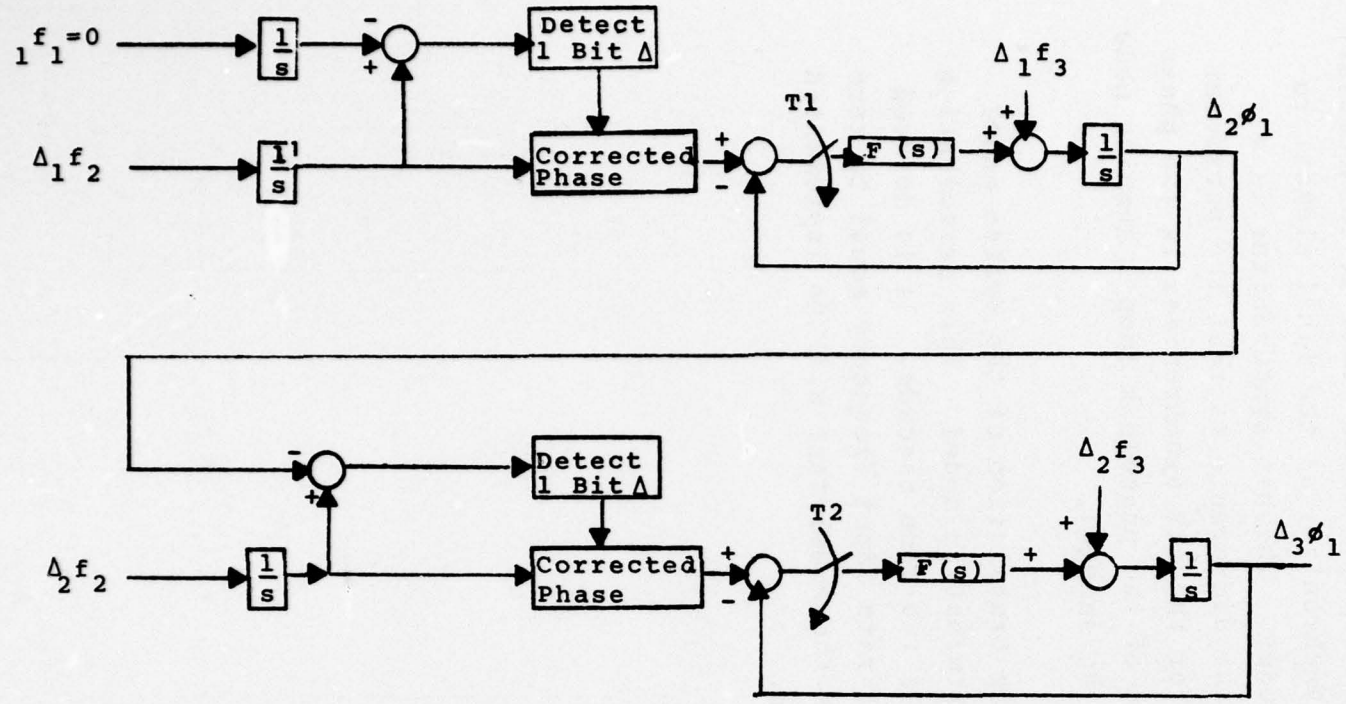


Figure 2
System Perturbation Model

AD-A049 310 HARRIS CORP MELBOURNE FLA ELECTRONIC SYSTEMS DIV F/G 17/2
ANALYSIS OF JITTER CHARACTERISTICS IN A PULSE STUFFING TDM NETW--ETC(U)
JUN 77 J A GRACIA, T G ZOGAKIS DCA100-76-C-0072
UNCLASSIFIED SBIE-AD-E100 005 NL

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Simulation Objective

The simulation objective is to obtain answers to the pulse stuffing jitter problems by conducting simulation experiments such as those shown below:

a) Measurement of "waiting-time" jitter for the same stuffing ratio, ρ, derived by using different values of frequency of stuffing opportunities (frame length) vs T2 rate (offset frequency) and using a single-node and positive stuffing system.

b) Measurement of "waiting-time" jitter for different stuffing ratios, ρ, using a single-node and positive stuffing system.

c) Measurement of "waiting-time" jitter for the same stuffing ratio, ρ, derived by using different values of frequency of stuffing opportunities (frame length) vs T2 rate (offset frequency) and using a single-node and negative stuffing system.

d) Measurement of "waiting-time" jitter for different stuffing ratios, ρ, using a single-node and negative stuffing system.

e) Measurement of overall jitter smoothing for a given stuffing ratio by varying the cut-off frequency of a first-order smoothing loop for a single-node and positive stuffing system.

f) Measurement of overall jitter smoothing for a given stuffing ratio by varying the damping factor and natural frequency of a second-order smoothing loop for a single node and positive stuffing system.

g) Measurement of "waiting-time" jitter and "cascading" jitter for a given stuffing ratio using a first-order smoothing loop in a two-node positive stuffing system. This experiment must be iterated over varations in the phase relationship between the stuffing opportunities clock of each node.

h) Repeat the above experiment using three nodes instead of two. Measure the "waiting-time" and "cascading" jitter in an effort to verify the postulation that the impact of cascading is equal to or less than the RMS summing of the RMS jitter of each individual cascade.

i) Repeat the above experiment using two nodes and negative stuffing instead of positive stuffing.

j) Repeat the above experiment using three nodes and negative stuffing. Attempt to verify the effects of cascading is equal to summing the RMS jitter as shown for the positive stuffing case.

k) Repeat the experiment using multiple nodes and positive stuffing. Measure the RMS jitter for various combinations of phase relationship between the stuffing opportunities clock of each node. Use a first-order loop.

l) Repeat the above experiment using a second-order loop.

m) Add a second-order bit synchronizer to the simulation using the multiple cascade of the above experiment and measure the phase error. Attempt to determine the bit synchonizer optimum parameter by iterating them during the simulation.

To conduct the above simulation experiment it becomes necessary to measure the following parameters:

a) Peak jitter variations to determine buffer requirements.

b) RMS jitter variation to determine the effect of cascading multiple-nodes and effects of variation of jitter parameter.

c) Plots of instantaneous frequency vs time for the output to observe variations of peak to peak frequency jitter.

d) Plots of phase jitter vs time for the output to observe variations of peak to peak phase jitter.

e) Plots of frequency slew rate vs time at the summing node of the bit synchronizer to establish bit synchronizer requirements.

Program Description

Due to resource limitation the detailed program description has not been developed. The basic simulation has been developed and verified. Simulation experiments have been conducted and results have been included in the analysis effort.

The simulator is written in GASP IV which is a FORTRAN IV based simulation language. It consists of a main program and five subroutines. Four of these subroutines EVNTS, INTLC, SCOND, and STATE are required to interface this combined (discrete event-continuous) simulation to the GASP IV Subroutine Library. The fifth subroutine PHASE was needed to support the EVNTS, INTLC, and STATE subroutines. Figure 3 shows the functional flow interrelationship between these user written subroutines and the GASP IV Subroutine Library Package. Program listing of these subroutines are included to complete this description.

The software simulation was implemented to study the steady-state performance of a system with one to ten cascaded nodes. Each node contains a digital phase-lock loop and pulse stuffing simulation and the last node includes simulation of a bit synchronizer (receiver) as the terminating component. Since the system operates in the MHz region, a perturbational node model was developed to avoid numerical accuracy problems. The model of a node is a linear model (phase detector, VCO, etc.) which is valid for steady-state performance analysis. Steady-state as used implies hold-in performance as opposed to signal acquisition. This system has repeated transient impacts due to the pulse stuffing.

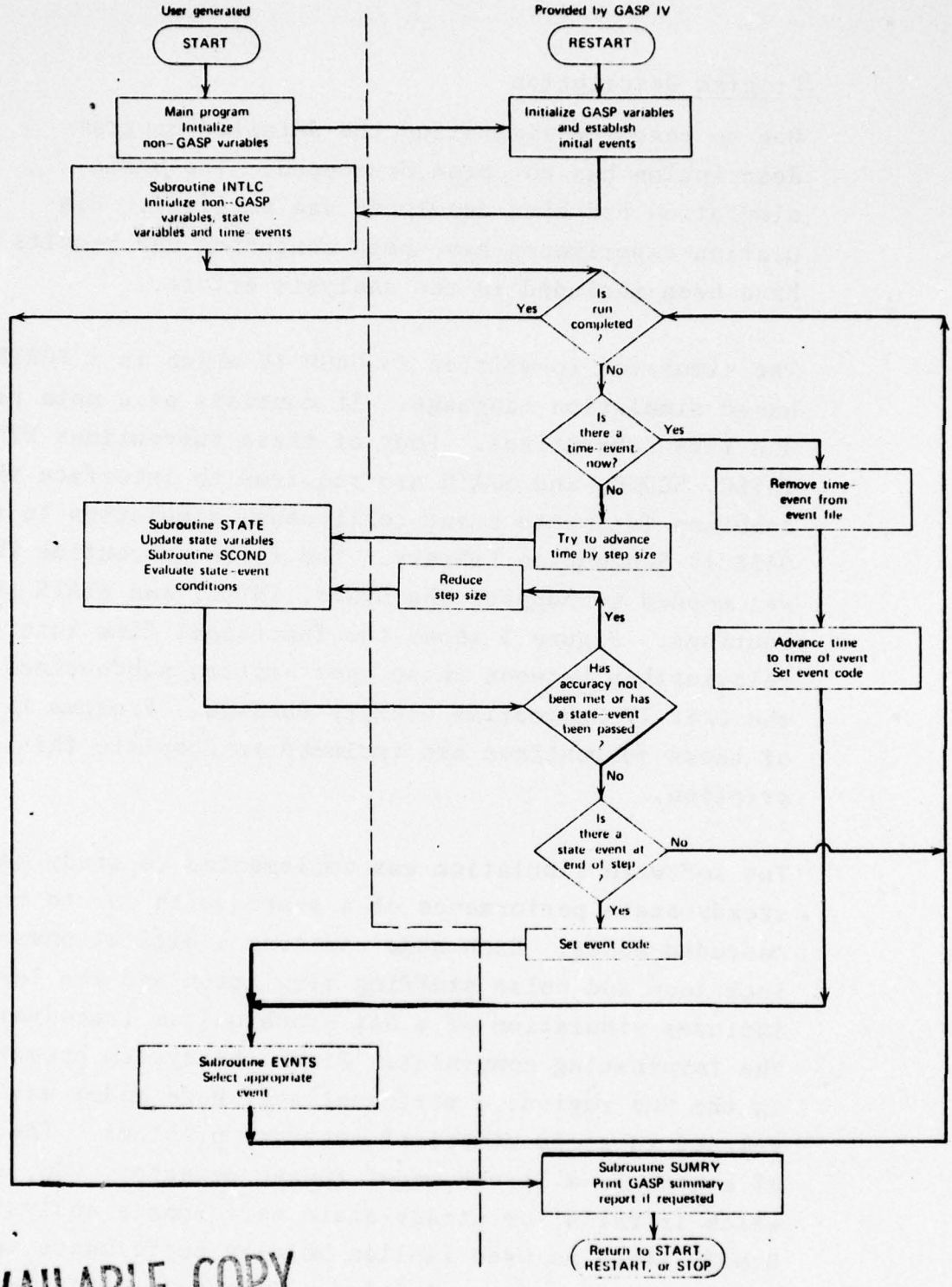

Figure 3. Functional Flow Between MUXJIT and GASP IV

The 'natural' simulation model implementation for a digital phaselock loop (PLL) is a discrete simulation; however, the system is highly oversampled (i.e., the PLL bandwidth is very low compared to the sample rate). This condition actually permitted the simulation model of the PLL to be implemented as a continuous system defined as differential equations to provide a faster solution on the computer with an identical dynamic response. The variable step size Runge-Kutta-England integration algorithm permitted relatively large time increments for integration after the transient from each pulse stuffing activity.

The dynamic equations are table-driven to permit generalized routines for first or second order nodes that are accessed based on the number of nodes being simulated for any one simulation run. Discrete events in the simulation include the opportunity to advance or retard the node phase and the periodic collection of phase and frequency statistics for analysis and plotting. Minimum and maximum phase peaks are detected which trigger a state-event for collection of statistics on peak phase variation.

```
C*****PULSE JITTER STUDY*************************************************
C
C      PURPOSE
C         STIMULATE CASCADED NODES FOR ANALYSIS OF WAITING TIME JITTER
C
C      DESCRIPTION OF PARAMETERS
C         DW2( ) - DATA TRANSFER FREQUENCY (RAD/SEC) AT EACH NODE.
C                  PERTURBATION FROM BASIC CHANNEL FREQUENCY.
C         DW3( ) - VCO FREQUENCY (RAD/SEC) AT EACH NODE.
C                  PERTURBATION FROM BASIC CHANNEL FREQUENCY.
C         GAIN( )- GAIN OF PHASELOCK LOOP.
C         TAU( ) - TIME CONSTANT FOR SECOND ORDER PHASELOCK LOOP.
C         PHERR( )-SAMPLED PHASE ERROR (RAD).
C         TS( )  - TIME BETWEEN SAMPLES FOR PHASELOCK LOOP. PERIOD OF
C                  SYNC FREQUENCY FOR EACH NODE.
C         NED( ) - FIXED DELAY IN PHASELOCK LOOP CORRECTION.
C                  DELAY WITHIN FRAME IN BITS.
C         CHFREQ - CHANNEL FREQUENCY.
C         NBPO   - NUMBER OF BITS PER OPPORTUNITY.
C         NFCUR  - CURRENT FRAME BEING PROCESSED.
C         NFSTRT - STARTING FRAME FOR DATA COLLECTION.
C         NFSTP  - STOPPING FRAME FOR DATA COLLECTION.
C         DTF    - TIME INCREMENT USED TO DETERMINE FSLEW.
C         NSPF   - NUMBER OF SAMPLES PER FRAME.
C         IDECSN - FLAG FOR DECISION TIME. RESET BY SAVE EVENT.
C
C      SYSTEM EVENTS
C         SAVE   - SAVE TIME FOR DATA.
C                  EVENT OCCURS EVERY SAVE TIME DTSAV.
C                  EVENT CODE 1.
C         DCRCT  - OPPORTUNITY TO DECIDE TO CORRECT PHASE OF SYNC
C                  FREQUENCY FOR NODE. OCCURS EVERY NBPF BITS.
C                  EVENT CODE 2.
C         CRCTN  - TIME TO CORRECT PHASE OF SYNC FREQUENCY FOR NODE.
C                  THIS EVENT GENERATED FROM DCRCT EVENT.
C                  EVENT CODE 3.
C         SEVNT  - STATE EVENT. DETECTION OF OUTPUT PHASE MINIMUM
C                  OR MAXIMUM. EVENT CODE 4.
C         FSAVE  - SAVE FREQUENCY TO DETERMINE FSLEW.
C                  EVENT CODE 5.
C
C      FILES
C         FILE 1 - EVENT FILE.
C                  ATRIB(1) - TIME OF EVENT.
C                  ATRIB(2) - EVENT CODE.
C                  ATRIB(3) - NODE INVOLVED IN EVENT ACTIVITY.
C
C      DATA COLLECTION
C         COLCT.
C            1 - PHMAX.
C            2 - PHMIN.
C         TIMSA.
C            1 - PHOUT.
C            2 - FNODE.
C            3 - FSLEW.
C            4 - PHERRN.
C            5 - PHTRK.
C            6 - PHSRCE.
```

```
C          HISTOGRAMS
C             1 - PHMAX.
C             2 - PHMIN.
C             3 - PHOUT.
C             4 - PHERRN.
C             5 - PHTRK.
C             6 - PHSRCE.
C             7 - FNODE.
C             8 - FSLEW.
C          PLOTS
C           PLOT 1.
C             3 - PHOUT.
C             4 - PHSRCE.
C             5 - PHERRN.
C             6 - PHTRK.
C           PLOT 2.
C             1 - FNODE.
C             2 - FSLEW.
C
C      REMARKS
C         THIS MODEL IS A PERTURBATIONAL MODEL.
C         DATA IS COLLECTED AT LAST NODE IN CASCADE.
C
C      SUBPROGRAMS REQUIRED
C         INTLC.EVNTS.STATE.PHASE + GASP SUBPROGRAMS
C
C*****************************************************************************
C
       NAME MUXJTT
C
C      PROGRAM DATE 770221
C
       COMMON QSET(200)
       COMMON /GCOM1/ ATRIB(25),JEVNT,MFA,MFE(100),MLE(100),MSTOP,NCRDR,N
      1NAPO,NNAPT,NNATR,NNFIL,NNQ(100),NNTRY,NPRNT,PPARM(50,4),TNOW,TTREG
      2,TTCLR,TTFIN,TTRIB(25),TTSET
       COMMON /SYSTEM/ NODES,NTYPE,DW2(11),DW3(11),GAIN(11),TAU(11),
      1 PHERR(11),NFD(11),TS(11),
      1 TPI,NAPO,NFSTRT,NFSTP,NFCUR,DTSAVE,DTF,IDECSN,NSPF,INIT
C
       TPI = 6.283185
       NCRDR=7
       NPRNT=6
C
       CALL GASP
       CALL EXIT
C
       END
```

SIZE 25 00031

```
C*****SUBROUTINE EVNTS*************************************************
C
C      PURPOSE
C         PROCESS SIMULATION EVENTS
C
C      DESCRIPTION OF PARAMETERS
C         NSYNC  - POINTER TO NODE N SYNC PHASE STATE.
C         NPHSE  - POINTER TO NODE N OUTPUT PHASE STATE.
C         NSRCE  - POINTER TO NODE N SOURCE PHASE STATE.
C         NINT   - POINTER TO NODE N INTERMEDIATE STATE.
C         PHSRCE - PHASE OF NODE N SOURCE.
C         PHSYNC - PHASE OF NODE N SYNC.
C         PHOUT  - PHASE OF NODE N OUTPUT.
C         PHERRN - PHASE OF NODE N ERROR.
C         PHTRK  - PHASE OF TRACKING LOOP ERROR.
C         FNODE  - FREQUENCY OF NODE N VCO.
C         FSLEW  - RATE OF CHANGE OF FREQUENCY OF NODE N VCO.
C
C      SUBPROGRAMS REQUIRED
C         STATE,PHASE + GASP SUBPROGRAMS
C
C**********************************************************************
C
      SUBROUTINE EVNTS(IX)
C
C      SUBROUTINE DATE 770221
C
      DOUBLE PRECISION LLARC,LLARH,LLARP,LLART
      COMMON /GCOM1/ ATRIB(25),JEVNT,MFA,MFE(100),MLE(100),MSTOP,NCRDR,N
     1NAPO,NNAPT,NNATR,NNFIL,NNQ(100),NNTRY,NPRNT,PPARM(50,4),TNOW,TTREG
     2,TTCLR,TTFIN,TTRIB(25),TTSET
      COMMON /GCOM2/ DD(100),DDL(100),DTFUL,DTNOW,ISEES,LFLAG(50),NFLAG,
     1NNEQD,NNEQS,NNEXT,SS(100),SSL(100),TTNEX
      COMMON /GCOM3/ AAERR,DTMAX,DTMIN,DTSAV,IITES,LLERR,LLSAV,LLSEV,RKE
     1RR,TTLAS,TTSAV
      COMMON /GCOM4/ DTPLT(10),HHIGW(25),HHWID(25),IICRO,IITAP(10),JJCEL
     1(500),LIARC(25,2),LLARH(25,2),LIARP(11,2),LLART(25,2),LIPHI(10),LL
     2PLO(10),LLPLT,LLSUP(15),LISYM(10),MMPTS,NNCEL(25),NNCLT,NNHIS,NNPL
     3T,NNPTS(10),NNSTA,NNVAR(10),PPHT(10),PPLO(10)
      COMMON /GCOM5/ EENQ(100),TTNN(100),KKRNK(100),MMAXQ(100),QQTIM(100
     1),SSQRV(25,5),SSTPV(25,6),VVNQ(100)
      COMMON /SYSTEM/ NODES,NTYPE,DW2(11),DW3(11),GAIN(11),TAU(11),
     1 PHERR(11),NFD(11),TS(11),
     1 TPI,NRPO,NFSTRT,NFSTP,NFCUR,DTSAVE,DTF,IDECSN,NSPF,INIT
      DIMENSION XX(10)
C
C      *****
C      *
C******      DETERMINE NODE FOR EVENT ACTIVITY AND ESTABLISH
C      *      CORRECT POINTERS FOR PHASE
C      *
C      *****
C
      N = ATRIB(3)
      IF (IX .EQ. 4) N = NODES
      CALL STATE
      CALL PHASE(NTYPE,N,NSYNC,NPHSE,NINT,PHSYNC,PHOUT,PHINT,PHSRCE)
C
```

```
C      *****
C      *
C******              PROCESS EVENT CODE TX
C      *
C      *****
C
       GO TO (1000,2000,3000,4000,5000), TX
C
C      *****
C      *
C******              SAVE
C      *
C      *****
C
 1000 CONTINUE
C
C******              SAVE DATA FOR PLOTTING AND STATISTICS COLLECTION
C      *             AT REGULAR INTERVALS
C
       TSAVE = TNOW
       PHSRCE = PHSRCE * 360.0 / TPI
       PHSYNC = PHSYNC * 360.0 / TPI
       PHOUT = PHOUT * 360.0 / TPI
       PHERRN = PHSYNC - PHOUT
       PHTRK = PHOUT - SS(NNEQ0-1) * 360.0 / TPI
       FNODE = DD(NPHSE) / TPI
C
       IF (INIT .EQ. 0) GO TO 1010
C
C******              FIRST SAVE TIME
C      *             CLEAR STATISTICAL ARRAYS AND INITIALIZE
C
       CALL CLEAR
       SSTPV(1,6) = PHOUT
       SSTPV(4,6) = PHERRN
       SSTPV(5,6) = PHTRK
       SSTPV(6,6) = PHSRCE
C
 1010 CONTINUE
C
       IF (NNPLT .EQ. 0) GO TO 1100
C
C******              STORE DATA FOR PLOTTING
C
       XX(1) = IDECSN
       XX(2) = PHSYNC
       XX(3) = PHOUT
       XX(4) = PHSRCE
       XX(5) = PHERRN
       XX(6) = PHTRK
       IDECSN = 0
       CALL GPLOT(XX,TNOW,1)
C
 1100 CONTINUE
       IF (NNSTA .GT. 0) CALL TIMSA(PHOUT,TNOW,1)
       IF (NNSTA .GT. 3) CALL TIMSA(PHERRN,TNOW,4)
       IF (NNSTA .GT. 4) CALL TIMSA(PHTRK,TNOW,5)
       IF (NNSTA .GT. 5) CALL TIMSA(PHSRCE,TNOW,6)
```

```
      IF (NNHIS .GT. 2) CALL HISTO(PHOUT,3)
      IF (NNHIS .GT. 3) CALL HISTO(PHERRN,4)
      IF (NNHIS .GT. 4) CALL HISTO(PHTRK,5)
      IF (NNHIS .GT. 5) CALL HISTO(PHSRCE,6)
C
C******            SCHEDULE NEXT FREQUENCY SAVE TIME TO GET FSLEW
C
      ATRIB(1) = TNOW + DTF
      ATRIB(2) = 5.0
      CALL FTLEM(1)
      RETURN
C
C     *****
C     *
C******            DCRCT
C     *
C     *****
C
 2000 CONTINUE
      IF (N .EQ. NODES) NECUR = NECUR + 1
      IF (NECUR .GT. NESTP) MSTOP = -1
C
C******            SCHEDULE NEXT DECISION FOR CORRECTION
C
      ATRIB(1) = TNOW + NRPO * TS(N)
      CALL FTLEM(1)
C
      IDECSN = 1
      IF ((NECUR .LT. NESTRT) .OR. (N .NE. NODES)) GO TO 2500
C
C******            CREATE NSPF SAVE TIMES FOR THIS FRAME
C
      ATRIB(2) = 1.0
      ATRIB(3) = N
      ATRIB(4) = 0.0
      DO 2100 I = 1,NSPF
      ATRIB(1) = TNOW + (I - 1) * DTSAVE + NED(N) * TS(N)
      CALL FTLEM(1)
 2100 CONTINUE
C
C******            TEST FOR 1 BIT ERROR BETWEEN SOURCE CHANNEL AND
C     *             FREQUENCY SOURCE PHASE
C
 2500 CONTINUE
      ERR = PHSYNC - PHSRCE
      IF (ABS(ERR) .LT. TPI) RETURN
C
C******            SCHEDULE PHASE CORRECTION
C     *             ATTRIBUTE 4 IS THE CORRECTION TO BE MADE
C     *             CORRECT PHASE IMMEDIATELY IF NED(N) = 0
C
      ATRIB(4) = SIGN(TPI,ERR)
      IF (NED(N) .EQ. 0) GO TO 3000
      ATRIB(1) = TNOW + NED(N) * TS(N)
      ATRIB(2) = 3
      CALL FTLEM(1)
      RETURN
C
```

```
C      *****
C      *
C******              CRCTN
C      *
C      *****
C
 3000 CONTINUE
C
C******              CORRECT PHASE OF SYNC FREQUENCY FOR NODE N
C
       SS(NSYNC) = SS(NSYNC) - ATBTR(4)
       RETURN
C
C      *****
C      *
C******              STATE EVENT
C      *
C      *****
C
 4000 CONTINUE
       PHOUT = PHOUT * 360.0 / TPI
       IF (IFLAG(1) .EQ. 0) GO TO 4010
C      PHASE MAXIMUM
       IF (NNHIS .GT. 0) CALL HISTO(PHOUT,1)
       IF (NNCLT .GT. 0) CALL COLCT(PHOUT,1)
       RETURN
C
 4010 CONTINUE
       IF (IFLAG(2) .EQ. 0) GO TO 4020
C      PHASE MINIMUM
       IF (NNHIS .GT. 1) CALL HISTO(PHOUT,2)
       IF (NNCLT .GT. 1) CALL COLCT(PHOUT,2)
C
 4020 CONTINUE
       RETURN
C
C      *****
C      *
C******              FREQUENCY SAVE EVENT
C      *
C      *****
C
 5000 CONTINUE
       FSLEW = (DD(JPHSE) / TPI - FNODE) / (TNOW - TSAVE)
       IF (INIT .EQ. 0) GO TO 5010
       INIT = 0
       SSTPV(2,6) = FNODE
       SSTPV(3,6) = FSLEW
C
 5010 CONTINUE
       IF (NNPLT .EQ. 1) GO TO 5100
C
C******              STORE DATA FOR PLOTTING
C
       XX(1) = FNODE
       XX(2) = FSLEW
       CALL GPLOT(XX,TSAVE,2)
C
```

```
5100 CONTINUE
     IF (NNSTA .GT. 1) CALL TIMSA(ENODE,TSAVE,2)
     IF (NNSTA .GT. 2) CALL TIMSA(ESLEW,TSAVE,3)
     IF (NNHIS .GT. 5) CALL HISTO(ENODE,7)
     IF (NNHIS .GT. 7) CALL HISTO(ESLEW,8)
     RETURN
C
     END
```

SIZE 568 01070

```
C*****SUBROUTINE INTLC*************************************************
C
C      PURPOSE
C         INITIALIZE SYSTEM
C
C      REMARKS
C         CODE IS INCLUDED TO INTITALIZE SYSTEM IN STEADY STATE.
C
C      SUBPROGRAMS REQUIRED
C         PHASE + GASP SUBPROGRAMS
C
C************************************************************************
C
      SUBROUTINE INTLC
C
C      SUBROUTINE DATE 770221
      DIMENSION PSYNC(11),POUT(11)
C
      DOUBLE PRECISION LLABC,LLABH,LLABP,LLABT
      COMMON /GCOM1/ ATRIB(25),JEVNT,MFA,MFE(100),MLE(100),MSTOP,NCRDR,N
     1NAPQ,NNAPT,NNATR,NNFIL,NNQ(100),NNTRY,NPRNT,PPARM(50,4),TNOW,TTREG
     2,TTCLR,TTFIN,TTRIB(25),TTSET
      COMMON /GCOM2/ DD(100),DDL(100),DTFUL,DTNOW,ISEED,LFLAG(50),NFLAG,
     1NNEQD,NNEQS,NNEQT,SS(100),SSL(100),TTNEX
      COMMON /GCOM3/ AAERR,DTMAX,DTMIN,DTSAV,IITES,LLERR,LLSAV,ILSEV,RKE
     1RR,TTLAS,TTSAV
      COMMON /GCOM4/ DTPLT(10),HHIGH(25),HHWID(25),IICRD,IITAP(10),JJCEL
     1(500),LABC(25,2),LLABH(25,2),LLABP(11,2),LLABT(25,2),LIPHI(10),LL
     2PLO(10),LIPLT,LLSUP(15),LISYM(10),MMPTS,NNCEL(25),NNCLT,NNHIS,NNPL
     3T,NNPTS(10),NNSTA,NNVAR(10),PPHI(10),PPLO(10)
      COMMON /SYSTEM/ NODES,NTYPE,DW2(11),DW3(11),GAIN(11),TAU(11),
     1 PHERR(11),NFD(11),TS(11),
     1 TPI,NBPQ,NFSTRT,NFSTP,NFCUR,DTSAVE,DTF,IDECSN,NSPF,INIT
C
      WRITE(NPRNT,9700)
C
      NNEQD = 0
      NFCUR = 1
      READ(NCRDR,-) NFSTRT,NFSTP,NSPF
      WRITE(NPRNT,9100) NFSTRT,NFSTP
C
C      *****
C      *
C******              READ INPUT PARAMETERS AND CONVERT TO SIMULATION
C      *              INPUT FORMS
C      *
C      *****
C
C******              ENTER CHANNEL FREQUENCY IN MHZ AND NUMBER
C      *              OF BITS PER OPPORTUNITY
C
      READ(NCRDR,-) CHFREQ,NBPQ
      WRITE(NPRNT,9110) CHFREQ,NBPQ
C
C******              ENTER NUMBER OF NODES AND TYPE OF SYSTEM
C
      READ(NCRDR,-) NODES,NTYPE
      WRITE(NPRNT,9120) NODES,NTYPE
```

```
C
C******              ENTER PARAMETER SETS FOR EACH NODE
C
      DO 1000 N = 1,NODES
      WRITE(NPRNT,9130) N
C
C******              ENTER DATA TRANSFER FREQUENCY IN MHZ, FIXED DELAY
C     *              IN BITS AND VCO NOMINAL FREQUENCY IN MHZ
C
      READ(NCRDR,*) F2,NFD(N),F3
      WRITE(NPRNT,9140) F2,NFD(N),F3
      TS(N) = 1.0 / (F2 * 1.0E6)
      DW2(N) = 1.0E6 * (F2 - CHFREQ) * TPI
      DW3(N) = 1.0E6 * (F3 - CHFREQ) * TPI
C
C******              ENTER SYNC PHASE AND OUTPUT PHASE IN DEG
C
      READ(NCRDR,*) PSYNC(N),POUT(N)
      WRITE(NPRNT,9145) PSYNC(N),POUT(N)
      PSYNC(N) = PSYNC(N) * TPI / 360.0
      POUT(N) = POUT(N) * TPI / 360.0
C
C******              LOOP BANDWIDTH IN HZ AND DAMPING (SECOND ORDER ONLY)
C
      IF (NTYPE .EQ. 2) GO TO 100
C
C     FIRST ORDER LOOP
C
      READ(NCRDR,*) FN
      WRITE(NPRNT,9150) FN
      WN = TPI * FN
C     CONVERT BANDWIDTH INPUT TO GAIN FOR SIMULATION
      GAIN(N) = WN
      NNEQD = NNEQD + 2
      GO TO 200
C
C     SECOND ORDER LOOP
C
  100 CONTINUE
      READ(NCRDR,*) FN,ZETA
      WRITE(NPRNT,9160) FN,ZETA
      WN = TPI * FN
C     CONVERT BANDWIDTH INPUT AND DAMPING TO GAIN AND TAU FOR SIMULATION
      GAIN(N) = WN * WN
      TAU(N) = 2 * ZETA / WN
      NNEQD = NNEQD + 3
C
  200 CONTINUE
C
 1000 CONTINUE
C
C     *****
C     *
C******              TRACKING LOOP PARAMETERS
C     *
C     *****
C
C
```

```
C******              ENTER VCO NOMINAL FREQUENCY IN MHZ
C
      READ(NCRDR,*) F3
      WRITE(NPRNT,9170) F3
      DW3(N) = 1.0E6 * (F3 - CHFREQ) * TPI
C
C******              ENTER LOOP BANDWIDTH IN HZ AND DAMPING
C
      READ(NCRDR,*) FN,ZETA
      WRITE(NPRNT,9160) FN,ZETA
      WN = TPI * FN
C     CONVERT BANDWIDTH INPUT AND DAMPING TO GAIN AND TAU FOR SIMULATION
      GAIN(N) = WN * WN
      TAU(N) = 2 * ZETA / WN
      NNEQD = NNEQD + 2
      NNEQT = NNEQD
C
C     *****
C     *
C******              INITIALIZE SYSTEM EVENTS
C     *
C     *****
C
      DO 2000 N = 1,NODES
      CALL PHASE(NTYPE,N,NSYNC,NPHSE,NINT,PHSYNC,PHOUT,PHINT,PHSRCE)
      IF (NTYPE .EQ. 2) GO TO 1100
C
C     FIRST ORDER SYSTEM
C
C     INITIALIZE PHASES
      SS(NSYNC) = PHSRCE + PSYNC(N)
      SS(NPHSE) = SS(NSYNC) + POUT(N)
      GO TO 1200
C
C     SECOND ORDER SYSTEM
C
 1100 CONTINUE
C     INITIALIZE PHASES
      SS(NSYNC) = PHSRCE + PSYNC(N)
      SS(NPHSE) = SS(NSYNC) + POUT(N)
      SS(NINT) = -DW3(N) / GAIN(N)
 1200 CONTINUE
      PHERR(N) = 0.0
C
C******              SCHEDULE FIRST DCRCTN TIME
C
      ATRIB(1) = 0.0
      ATRIB(2) = 2.0
      ATRIB(3) = N
      ATRIB(4) = 0.0
      CALL FILEM(1)
 2000 CONTINUE
C
      N = NODES + 1
      NINPUT = NPHSE
      NPHSE = NNEQD - 1
      NINT = NNEQD
      SS(NPHSE) = SS(NINPUT)
```

```
      SS(NINT) = -D#3(N) / GAIN(N)
      IDECSN = 0
      INIT = 1
      DTSAVE = NBPO * TS(NODES) / NSPF
      DTPLT(1) = DTSAVE
      DTPLT(2) = DTSAVE
      DTF = 0.1 * TS(NODES)
      RETURN
9100 FORMAT(10X,'DATA COLLECTION STARTS AT FRAME',I4,
     1 1X,'AND STOPS AT FRAME',I4)
9110 FORMAT(///,10X,'T1 FREQUENCY SOURCE =',1PE15.7,1X,'MHZ'/
     1 10X,'NUMBER OF BITS PER OPPORTUNITY =',I4)
9120 FORMAT(///,10X,'SYSTEM PARAMETERS FOR',I3,1X,'NODES'/
     1 10X,'ALL NODES ARE TYPE',I2,1X,'SYSTEMS')
9130 FORMAT(//,10X,'NODE',I3)
9140 FORMAT(/,10X,'T2 FREQUENCY SOURCE =',1PE15.7,1X,'MHZ'/
     1 10X,'CORRECTION APPLIED IN BIT',I3,1X,'OF FRAME'/
     1 10X,'VCO NOMINAL FREQUENCY =',1PE15.7,1X,'MHZ')
9145 FORMAT(/,10X,'T2 INITIAL PHASE =',F5.0,1X,'DEG'/
     1 10X,'NODE OUTPUT PHASE =',F5.0,1X,'DEG')
9150 FORMAT(/,10X,'NATURAL FREQUENCY (FN) =',1PE15.7,1X,'HZ')
9160 FORMAT(/,10X,'NATURAL FREQUENCY (FN) =',1PE15.7,1X,'HZ'/
     1 10X,'DAMPING (ZETA) =',0PF5.3)
9170 FORMAT(///,10X,'TRACKING LOOP PARAMETERS'/
     1 10X,'VCO NOMINAL FREQUENCY =',1PE15.7,1X,'MHZ')
9700 FORMAT('1')
      END
```

SIZE 950 01666

```
C*****SUBROUTINE SCOND*****
C
C      PURPOSE
C         DETECT MINIMUM AND MAXIMUM PHASE PEAKS AT LAST NODE IN CASCADE
C
C      REMARKS
C         PHASE MIN AND MAX DETECTED WITHIN TWO DEGREES.
C
C      SUBPROGRAMS REQUIRED
C         GASP SUBPROGRAMS
C*****
C
      SUBROUTINE SCOND
C
C      SUBROUTINE DATE 770110
C
      COMMON /GCOM1/ ATRIB(25),JEVNT,MFA,MFE(100),MLE(100),MSTOP,NCRDR,N
     1NAPO,NNAPT,NNATR,NNFIL,NNQ(100),NNTRY,NPRNT,PPARM(50,4),TNOW,TTREG
     2,TTCLR,TTFIN,TTRIB(25),TTSET
      COMMON /GCOM2/ DD(100),DDL(100),DTFUL,DTNOW,ISEES,LFLAG(50),NFLAG,
     1NNEQD,NNEQS,NNEQT,SS(100),SSL(100),TTNEX
      COMMON /SYSTEM/ NODES,NTYPE,DW2(11),DW3(11),GAIN(11),TAU(11),
     1 PHERR(11),NFD(11),TS(11),
     1 TPI,NRPO,NFSTRT,NFSTP,NFCUR,DTSAVE,DTF,IDECSN,NSPF,INIT
C
      GO TO (100,200), NTYPE
C
  100 CONTINUE
C     FIRST ORDER SYSTEM
      NPHSE = 2 * NODES
      GO TO 300
  200 CONTINUE
C     SECOND ORDER SYSTEM
      NPHSE = 3 * NODES - 1
  300 CONTINUE
      LFLAG(1) = KROSS(-NPHSE,0.0,0.0,-1.100.0)
      LFLAG(2) = KROSS(-NPHSE,0.0,0.0,1.100.0)
C
      RETURN
      END
```

SIZE 70 00106

```
C*****SUBROUTINE STATE*****
C
C     PURPOSE
C        CALCULATE SYSTEM STATE DERIVATIVES
C
C     REMARKS
C        THE SYSTEM IS A CASCADE OF NODES FOLLOWED BY A TRACKING LOOP.
C        ALL NODES IN CASCADE ARE THE SAME TYPE (FIRST OR SECOND ORDER).
C        THE TRACKING LOOP IS A SECOND ORDER LOOP.
C
C     SUBPROGRAMS REQUIRED
C        NONE
C
C*****
C
      SUBROUTINE STATE
C
C     SUBROUTINE DATE 770221
C
      COMMON /GCOM1/ ATRIB(25),IEVNT,MFA,MFE(100),MLF(100),MSTOP,NCRDR,N
     1NAPO,NNAPT,NNATR,NNFIL,NNQ(100),NNTRY,NPRNT,PPARM(50,4),TNOW,TTBEG
     2,TTCLR,TTFIN,TTRIB(25),TTSET
      COMMON /GCOM2/ DD(100),DDL(100),DTFUL,DTNOW,ISEED,LFLAG(50),NFLAG,
     1NNEQD,NNEQS,NNEQT,SS(100),SSL(100),TTNEX
      COMMON /SYSTEM/ NODES,NTYPE,DW2(11),DW3(11),GAIN(11),TAU(11),
     1 PHERR(11),NFD(11),TS(11),
     1 TPI,NRPO,NFSTRT,NFSTP,NFCUR,DTSAVE,DTF,IDECSN,NSPF,INIT
C
C     *****
C     *
C*****            SOLVE FIRST OR SECOND ORDER SYSTEM EQUATIONS
C     *            FOR ALL NODES
C     *
C     *****
C
      IF (NTYPE .EQ. 2) GO TO 1000
C
C*****            FIRST ORDER SYSTEM EQUATIONS
C
      DO 100 N = 1,NODES
      NSYNC = 2*N - 1
      NPHSE = NSYNC + 1
      PHERR(N) = SS(NSYNC) - SS(NPHSE)
      DD(NSYNC) = DW2(N)
      DD(NPHSE) = GAIN(N) * PHERR(N) + DW3(N)
  100 CONTINUE
C
      GO TO 2000
C
C*****            SECOND ORDER SYSTEM EQUATIONS
C
 1000 CONTINUE
      DO 1100 N = 1,NODES
      NSYNC = 3 * N - 2
      NPHSE = NSYNC + 1
      NINT = NPHSE + 1
      PHERR(N) = SS(NSYNC) - SS(NPHSE)
      DD(NSYNC) = DW2(N)
```

```
      DD(NPHSE) = GAIN(N) * (TAU(N) * PHERR(N) + SS(NINT)) + DW3(N)
      DD(NINT) = PHERR(N)
 1100 CONTINUE
C
C     *****
C     *
C*****            TRACKING LOOP
C     *
C     *****
C
 2000 CONTINUE
C
C*****            SET UP POINTERS FOR TRACKING LOOP
C
      N = NODES + 1
      NINPUT = NPHSE
      NPHSE = NNEQD - 1
      NINT = NNEQD
      PHERR(N) = SS(NINPUT) - SS(NPHSE)
      DD(NPHSE) = GAIN(N) * (TAU(N) * PHERR(N) + SS(NINT)) + DW3(N)
      DD(NINT) = PHERR(N)
      RETURN
      END
```

SIZE 265 00411

```
C*****SUBROUTINE PHASE*****
C
C      PURPOSE
C         DETERMINE POINTERS AND CURRENT VALUES FOR NODE SYNC AND
C         OUTPUT PHASE BASED ON TYPE OF NODE AND NODE NUMBER
C
C      SUBPROGRAMS REQUIRED
C         NONE
C
C*****
C
      SUBROUTINE PHASE(NTYPE,NODE,NSYNC,NPHSE,NINT,PHSYNC,PHOUT,PHINT,
     1 PHSRCE)
C
C      SUBROUTINE DATE 761214
C
      COMMON /GCOM2/ DD(100),DDI(100),DTFUL,DTNOW,ISEES,LFLAG(50),NFLAG,
     1NNEQD,NNEQS,NNEQT,SS(100),SSL(100),TTNEX
C
      PHSRCE = 0.0
C
      GO TO (100,200), NTYPE
C
C      FIRST ORDER SYSTEM
C
  100 CONTINUE
      NSYNC = 2 * NODE - 1
      NPHSE = NSYNC + 1
      NSRCE = NSYNC - 1
      PHSYNC = SS(NSYNC)
      PHOUT = SS(NPHSE)
      IF (NSRCE .GT. 0) PHSRCE = SS(NSRCE)
      RETURN
C
C      SECOND ORDER SYSTEM
C
  200 CONTINUE
      NSYNC = 3 * NODE - 2
      NPHSE = NSYNC + 1
      NSRCE = NSYNC - 1
      NINT = NPHSE + 1
      PHSYNC = SS(NSYNC)
      PHOUT = SS(NPHSE)
      PHINT = SS(NINT)
      IF (NSRCE .GT. 0) PHSRCE = SS(NSRCE)
      RETURN
C
```

APPENDIX C

DATA SHEETS FOR EXPERIMENTS PERFORMED IN PHASE II - TEST AND EVALUATION

The data that appear in this Appendix were collected during the test and evaluation phase of this study. These readings were taken directly off the equipment located in the second level multiplexer simulator test bed facility. The reader is referred to Subsection 6.3 for a description of the test setup and equipment configuration. These data were used in Subsection 6.4 to describe and explain the thirteen experiments performed for this study.

There are 15 tables that appear in this Appendix. Each table(s) corresponds to an experiment in the test matrix, which was described in Subsection 6.2.

Table C-1. Measured Test Control Parameters for Test 1

Sheet 1 of 1

T1 Frequency (MHz)	T1S Frequency (MHz)	BPO	ρ	Delay	Bandwidth (Hz)
1.543996	1.545800	288	.335	0	1528
					764
					382
					191
					96

Table C-2. Jitter Data for Test 1

Sheet 1 of 1

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)
.260	1.180	61.5	279.0	1528
.190	.860	44.9	203.3	764
.149	.690	35.2	163.1	382
.130	.550	30.7	130.0	191
.116	.450	27.4	106.4	96
.100	.350	23.6	82.7	48

Table C-3. Measured Test Control Parameters for Test 2

Sheet 1 of 1

T1 Frequency (MHz)	T1S Frequency (MHz)	BPO	ρ	Delay	Bandwidth (Hz)
1.543996	1.544937	576	.349	0	764
					382
					191
					96
					48

Table C-4. Jitter Data for Test 2

Sheet 1 of 1

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)
.265	1240	62.6	293.1	764
.187	.910	44.2	215.1	382
.128	.620	30.3	146.6	191
.084	.430	19.6	101.7	96
.049	.270	11.6	63.8	48

Table C-5. Jitter Data for Test 3

Sheet 1 of 8

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.032	.200	7.6	47.3	96	86	.100
.029	.190	6.9	44.9		96	.112
.029	.170	6.9	40.2		106	.123
.022	.150	5.2	35.5		116	.135
.025	.160	5.9	37.8		126	.147
.025	.170	5.9	40.2		136	.158
.032	.180	7.6	42.6		146	.170
.037	.200	8.7	47.3		156	.182
.033	.195	7.8	46.1		166	.193
.077	.330	18.2	78.0		172	.200

Table C-5. Jitter Data for Test 3

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.030	.180	7.1	42.6	96	182	.212
.034	.200	8.0	47.3		192	.224
.034	.210	8.0	49.6		202	.235
.070	.320	16.5	75.7		212	.246
.040	.220	9.5	52.0		222	.259
.032	.190	7.6	44.9		232	.270
.036	.220	8.5	52.0		242	.281
.033	.220	7.8	52.0		252	.293
.043	.260	10.2	61.5		258	.300
.042	.260	9.9	61.5	↓	268	.312

Table C-5. Jitter Data for Test 3

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.066	.310	15.6	73.3	96	278	.324
.115	.460	27.2	108.7		288	.335
.052	.285	12.3	67.4		298	.347
.041	.250	9.7	59.1		308	.359
.041	.240	9.7	56.7		318	.370
.040	.230	9.5	54.4		328	.382
.051	.270	12.1	63.8		338	.394
.078	.350	18.4	82.7		344	.401
.044	.360	10.4	61.5		354	.412
.048	.270	11.3	63.8	↓	364	.424

Table C-5. Jitter Data for Test 3

Sheet 4 of 8

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.048	.270	11.3	63.8	96	374	.436
.052	.300	12.3	70.9		384	.447
.060	.300	14.2	75.7		394	.459
.075	.380	17.7	89.8		404	.470
.105	.450	24.8	106.4		414	.482
.166	.600	39.2	141.8		424	.494
.190	.680	44.9	160.8		430	.501
.130	.500	30.7	118.2		440	.512
.094	.440	22.2	104.0		450	.524
.076	.400	18.0	94.6		460	.536

Table C-5. Jitter Data for Test 3

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.067	.360	15.8	85.1	96	470	.547
.062	.350	14.7	82.7		480	.559
.072	.370	17.0	87.5		490	.571
.062	.330	14.7	78.0		500	.582
.071	.360	16.8	85.1		510	.594
.080	.380	18.9	99.8		515	.600
.063	.320	14.9	75.7		505	.611
.067	.340	15.8	90.4		535	.623
.067	.350	15.8	82.7		545	.635
.077	.400	18.2	94.6		555	.646

Table C-5. Jitter Data for Test 3

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.108	.440	25.5	104.0	96	565	.658
.125	.530	29.6	125.3		575	.669
.089	.440	21.0	104.0		585	.681
.076	.400	18.0	94.6		595	.693
.076	.400	18.0	94.6		601	.700
.078	.400	18.4	94.6		611	.712
.075	.410	17.7	96.9		621	.723
.080	.400	18.9	94.6		631	.735
.108	.500	25.5	118.2		641	.747
.093	.460	22.0	108.7		651	.758

Table C-5. Jitter Data for Test 3

Sheet 7 of 8

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.085	.460	20.4	108.7	96	661	.770
.087	.470	20.0	111.1		671	.781
.097	.490	22.9	115.8		681	.793
.110	.520	26.0	127.9		687	.800
.097	.490	22.9	115.8		697	.812
.104	.500	24.6	118.2		707	.823
.114	.540	27.0	127.7		717	.835
.114	.540	27.0	127.7		727	.846
.125	.560	29.6	132.4		737	.858
.129	.600	30.5	141.8		747	.870

Table C-5. Jitter Data for Test 3

Sheet 8 of 8

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.136	.610	32.2	144.2	96	757	.881
.148	.640	35.0	154.3	↓	767	.893
.150	.680	35.5	160.8	↓	773	.900

Table C-6. Jitter Data for Test 4

Sheet 1 of 14

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.034	.200	8.0	47.3	48	165	.100
.021	.150	5.0	35.5		175	.106
.028	.170	6.6	40.2		185	.112
.023	.150	5.4	35.5		195	.118
.038	.200	9.0	47.3		205	.124
.024	.160	5.7	37.8		215	.130
.025	.170	5.9	40.2		225	.136
.053	.240	12.5	56.7		235	.142
.024	.170	5.7	40.2		245	.148
.028	.180	6.6	42.6	↓	255	.154

Table C-6. Jitter Data for Test 4

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.026	.180	6.1	42.6	48	265	.160
.052	.250	12.3	59.1		275	.166
.027	.180	6.4	42.6		285	.172
.026	.170	6.1	40.2		295	.179
.027	.180	6.4	40.2		305	.185
.029	.190	6.9	44.9		315	.191
.047	.220	11.1	52.0		325	.197
.064	.300	15.1	70.9		330	.200
.035	.180	8.3	42.6		340	.206
.030	.190	7.1	44.9		350	.212

Table C-6. Jitter Data for Test 4

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.030	.180	7.1	42.6	48	360	.218
.034	.190	8.0	44.9		370	.224
.037	.200	8.7	47.3		380	.230
.038	.200	9.0	47.3		390	.236
.043	.220	10.2	52.0		400	.242
.085	.330	20.1	78.0		410	.248
.057	.270	13.5	63.8		420	.254
.038	.210	9.0	49.6		430	.260
.034	.210	8.0	49.6		440	.266
.036	.220	8.5	52.0		450	.272

Table C-6. Jitter Data for Test 4

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.031	.180	7.3	42.6	48	460	.279
.054	.270	12.8	63.8		470	.285
.034	.210	8.0	49.6		480	.291
.034	.210	8.0	49.6		490	.297
.043	.250	10.2	59.1		496	.300
.038	.225	11.3	53.2		506	.306
.043	.250	10.2	59.1		516	.312
.049	.260	11.6	61.5		526	.318
.069	.320	16.3	75.7		536	.324
.115	.400	27.20	94.6		546	.330

Table C-6. Jitter Data for Test 4

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.102	.380	24.1	89.8	48	556	.336
.065	.290	15.4	68.6		566	.342
.049	.260	11.6	61.5		576	.348
.043	.240	10.2	56.7		586	.354
.041	.220	9.7	52.0		596	.360
.040	.220	9.5	52.0		606	.366
.048	.240	11.3	56.7		616	.372
.041	.220	9.7	52.0		626	.379
.043	.220	10.2	52.0		636	.385
.045	.250	10.6	59.1		646	.391

Table C-6. Jitter Data for Test 4

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.068	.300	16.1	70.9	48	656	.397
.078	.340	18.4	80.4		661	.400
.050	.250	11.8	59.1		671	.406
.045	.250	10.6	59.1		681	.412
.045	.250	10.6	59.1		691	.418
.050	.270	11.8	63.8		701	.424
.055	.280	13.0	66.2		711	.430
.050	.290	11.8	68.6		721	.436
.055	.300	13.0	70.9		731	.442
.053	.300	12.5	70.9	↓	741	.448

Table C-6. Jitter Data for Test 4

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E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.060	.320	14.2	75.7	48	751	.454
.064	.340	15.1	80.4		761	.460
.069	.360	16.3	85.1		771	.466
.080	.380	18.9	89.8		781	.472
.096	.420	22.7	99.3		791	.479
.119	.460	28.1	108.7		801	.485
.150	.540	35.5	127.7		811	.491
.185	.590	43.7	139.5		821	.497
.165	.600	39.0	141.8		826	.500
.160	.570	37.8	134.8		836	.506

Table C-6. Jitter Data for Test 4

Sheet 8 of 14

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.129	.480	30.50	113.5	48	846	.512
.106	.470	25.1	111.1		856	.518
.091	.420	21.5	99.3		866	.524
.080	.400	18.9	94.6		876	.530
.072	.370	17.0	87.5		886	.536
.067	.350	15.8	82.7		896	.542
.064	.340	15.1	80.4		906	.548
.0666	.340	15.6	80.4		916	.554
.060	.340	14.2	80.4		926	.560
.062	.330	14.7	78.0		936	.566

Table C-6. Jitter Data for Test 4

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.067	.340	15.8	80.4	48	946	.572
.058	.325	13.7	76.8		956	.579
.058	.330	13.7	78.0		966	.585
.063	.335	14.9	79.2		976	.591
.081	.370	19.1	87.5		986	.597
.085	.370	20.1	87.5		991	.600
.019	.120	14.5	28.4		1001	.6006
.061	.300	14.4	70.9		1011	.612
.060	.325	14.2	76.8		1021	.618
.064	.330	15.1	78.0	↓	1031	.624

Table C-6. Jitter Data for Test 4

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.063	.330	14.9	78.0	48	1041	.630
.067	.350	15.8	82.7		1051	.636
.070	.370	16.5	87.5		1061	.642
.078	.380	18.4	89.8		1071	.648
.092	.410	21.7	96.9		1081	.654
.116	.460	27.4	108.7		1091	.660
.110	.500	26.0	118.2		1101	.666
.111	.450	26.2	106.4		1111	.672
.092	.400	21.7	94.6		1121	.679
.081	.400	19.1	94.6		1131	.685

Table C-6. Jitter Data for Test 4

Sheet 11 of 14

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.076	.400	18.0	94.6	48	1141	.691
.073	.370	17.3	87.5		1151	.697
.073	.390	17.3	92.2		1157	.700
.071	.370	16.8	87.5		1167	.706
.079	.380	18.7	89.8		1177	.712
.074	.370	17.5	87.5		1187	.718
.074	.390	17.5	92.2		1197	.724
.076	.400	18.0	94.6		1207	.730
.082	.420	19.4	99.3		1217	.736
.094	.440	22.2	104.0		1227	.742

Table C-6. Jitter Data for Test 4

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.100	.460	23.6	108.7	48	1237	.748
.099	.450	23.4	106.4		1247	.754
.087	.440	20.6	104.0		1257	.760
.083	.430	19.6	101.7		1267	.766
.083	.440	19.6	104.0		1277	.772
.085	.440	20.1	104.0		1287	.779
.086	.440	20.3	104.0		1297	.785
.087	.440	20.6	104.0		1307	.791
.105	.460	24.8	108.7		1317	.797
.100	.500	23.6	118.2	↓	1321	.800

Table C-6. Jitter Data for Test 4

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.097	.450	22.9	106.4	48	1331	.806
.095	.400	22.5	94.6		1341	.812
.097	.480	22.9	113.5		1351	.818
.100	.480	23.6	113.5		1361	.824
.110	.480	26.0	113.5		1371	.830
.110	.480	26.0	113.5		1381	.836
.108	.500	25.5	118.2		1391	.842
.111	.520	26.2	122.9		1401	.848
.118	.530	27.9	125.3		1411	.854
.120	.530	28.4	125.3	↓	1421	.860

Table C-6. Jitter Data for Test 4

Sheet 14 of 14

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)	BPO	ρ
.123	.570	29.1	134.8	48	1431	.866
.129	.560	30.5	132.4		1441	.872
.132	.570	31.2	134.8		1451	.879
.137	.580	32.4	137.1		1461	.885
.143	.600	33.8	141.8		1471	.891
.148	.620	35.0	146.6		1481	.897
.153	.650	36.2	153.7		1487	.900

Table C-7. Jitter Data for Test 5
ρ=.208

Sheet 1 of 1

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)
.275	1.160	65.0	224.2	382
.187	.880	44.2	208.0	191
.113	.540	26.7	127.7	96
.067	.350	15.8	82.7	48
.038	.215	9.0	50.8	24

Table C-8. Jitter Data for Test 6
ρ=.335

Sheet 1 of 1

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)
.260	1.200	61.5	283.7	1528
.198	.870	46.8	205.7	764
.157	.690	35.7	163.1	382
.130	.550	30.7	130.0	191
.115	.450	27.2	106.4	96
.085	.330	20.1	78.0	48

Table C-9. Jitter Data for Test 7
ρ=.335

Sheet 1 of 1

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)
.258	1.180	61.0	279.0	1528
.187	.860	44.2	203.3	764
.150	.690	35.5	163.1	382
.130	.540	30.7	127.7	191
.114	.440	27.0	104.0	96
.095	.330	22.5	78.0	48

Table C-10. Jitter Data for Test 8
σ=.349

Sheet 1 of 1

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)
.267	1.220	63.1	288.4	764
.186	.920	44.0	217.5	382
.129	.620	30.5	146.6	191
.085	.430	20.1	101.7	96
.051	.270	12.1	63.8	48

Table C-11. Jitter Data for Test 9
ρ=.349

Sheet 1 of 1

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	Bandwidth (Hz)
.260	1.200	61.5	283.7	76.4
.185	.930	43.7	219.9	382
.130	.660	30.7	156.0	191
.092	.470	21.7	111.1	96
.054	.300	12.8	70.9	48

Table C-12. Jitter Data for Test 10

Sheet 1 of 1

Test Step	E_o RMS (Volts)	E_o Peak-Peak (Volts)	Delay	Tandem	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)
1	.133	.545	2	1	31.4	128.8
2	.133	.545	4	1	31.4	128.8
3	.133	.545	8	1	31.4	128.8
4	.132	.540	12	1	31.2	127.7
5	.132	.550	2	3	31.2	130.0
6	.132	.545	4	3	31.2	128.8
7	.132	.545	8	3	31.2	128.8
8	.131	.540	12	3	31.0	127.7
9	.133	.545	2	1	31.4	128.8
10	.134	.550	8	2	31.7	130.0
11	.131	.540	4	3	31.0	127.7
12	.133	.550	0	1	31.4	130.0
13	.132	.545	2	2	31.2	128.8
14	.128	.525	10	3	30.3	124.1
15	.133	.550	10	1	31.4	130.0
16	.132	.545	2	2	31.2	128.8
17	.133	.545	0	3	31.4	128.8

Table C-13. Jitter Data for Test 11

Sheet 1 of 7

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	T1S (Mbps)	ρ
.240	.800	56.7	189.1	1.544107	.020
.186	.640	44.0	151.3	1.544160	.030
.106	.430	25.1	101.7	1.544322	.060
.084	.360	19.9	85.1	1.544429	.080
.075	.360	17.7	85.1	1.544536	.100
.068	.340	16.1	80.4	1.544586	.109
.061	.310	14.4	73.3	1.544636	.118
.060	.310	14.2	73.3	1.544686	.127
.056	.290	13.2	68.6	1.544736	.137
.055	.280	13.0	66.2	1.544786	.147
.050	.270	11.8	63.8	1.544836	.156
.068	.340	16.1	80.4	1.544886	.165
.049	.290	11.60	68.6	1.544936	.174
.048	.290	11.3	68.6	1.544986	.184
.051	.320	12.1	75.7	1.545036	.193

Table C-13. Jitter Data for Test 11

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	T1S (Mbps)	ρ
.031	.320	7.3	75.7	1.545073	.200
.045	.225	10.6	53.2	1.545123	.209
.044	.220	10.4	52.0	1.545173	.219
.042	.230	9.9	54.4	1.545223	.228
.046	.250	10.9	59.1	1.545273	.237
.075	.350	17.7	82.7	1.545323	.247
.061	.280	14.4	66.2	1.545373	.256
.041	.235	9.7	55.6	1.545423	.265
.039	.220	9.2	52.0	1.545473	.275
.049	.260	11.6	61.5	1.545523	.284
.038	.230	9.0	54.4	1.545573	.293
.030	.255	7.1	60.3	1.545610	.300
.041	.240	9.7	56.7	1.545660	.309
.051	.260	12.1	61.5	1.545710	.319
.087	.360	20.6	85.1	1.545760	.328

Table C-13. Jitter Data for Test 11

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	T1S (Mbps)	ρ
.100	.400	23.6	94.6	1.545810	.337
.054	.275	12.8	65.0	1.545860	.347
.042	.225	9.9	53.2	1.545910	.356
.041	215	9.7	50.8	1.545960	.365
.052	.265	12.3	62.6	1.546010	.374
.039	.200	9.2	47.3	1.546060	.384
.043	.220	10.2	52.0	1.546110	.393
.050	.300	11.8	70.9	1.546147	.400
.040	.235	9.5	55.6	1.546197	.409
.039	.220	9.2	52.0	1.546247	.418
.057	.270	13.5	63.8	1.546297	.428
.042	.225	9.9	53.2	1.546347	.437
.046	.235	10.9	55.6	1.546397	.447
.048	.255	11.3	60.3	1.546447	.456
.051	.260	12.1	61.5	1.546497	.465

Table C-13. Jitter Data for Test 11

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	T1S (Mbps)	ρ
.063	.290	14.9	68.6	1.546547	.475
.087	.360	20.6	85.1	1.546597	.484
.140	.520	33.1	122.9	1.546647	.493
.160	.560	37.8	132.4	1.546685	.500
.125	.470	29.6	111.1	1.546735	.509
.080	.320	18.9	75.7	1.546785	.519
.060	.290	14.2	68.6	1.546835	.528
.051	.260	12.1	61.5	1.546885	.537
.048	.250	11.3	59.1	1.546935	.547
.053	.275	12.5	65.0	1.546985	.556
.041	.230	9.7	54.4	1.547035	.565
.045	.235	10.7	55.6	1.547085	.575
.044	.230	10.4	54.4	1.547135	.584
.044	.240	10.4	56.7	1.547185	.593
.070	.310	16.5	73.3	1.547223	.600

Table C-13. Jitter Data for Test 11

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	T1S (Mbps)	ρ
.041	.220	9.7	52.0	1.547223	.610
.038	.200	9.0	47.3	1.547323	.619
.042	.220	9.9	52.0	1.547373	.628
.044	.230	10.4	54.4	1.547423	.638
.047	.240	11.1	56.7	1.547473	.647
.063	.295	14.9	69.7	1.547523	.656
.125	.440	29.6	104.0	1.547573	.665
.075	.340	17.7	80.4	1.547623	.675
.050	.260	11.8	61.5	1.547673	.684
.044	.270	10.4	56.7	1.547723	.693
.049	.265	11.6	62.6	1.547762	.700
.041	.230	9.7	54.4	1.547812	.709
.042	.240	9.9	56.7	1.547862	.719
.045	.240	10.6	56.7	1.547912	.728
.046	.245	10.9	57.9	1.547962	.737

Table C-13. Jitter Data for Test 11

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	T1S (Mbps)	ρ
.075	.340	17.7	80.4	1.548012	.747
.062	.310	14.7	73.3	1.548062	.756
.046	.260	10.9	61.5	1.548112	.765
.043	.230	10.2	54.4	1.548162	.774
.043	.235	10.2	55.6	1.548212	.783
.049	.270	11.6	63.8	1.548262	.793
.083	.360	19.6	85.1	1.548301	.800
.048	.265	11.3	62.6	1.548351	.810
.051	.270	12.1	63.8	1.548401	.819
.050	.270	11.8	63.8	1.548451	.828
.056	.285	13.2	67.4	1.548501	.838
.052	.275	12.3	65.0	1.548551	.847
.065	.320	15.4	75.7	1.548601	.856
.053	.265	12.5	62.6	1.548651	.865
.068	.330	16.1	78.0	1.548701	.875

Table C-13. Jitter Data for Test 11

Sheet 7 of 7

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	T1S (Mbps)	ρ
.059	.275	13.9	65.0	1.548751	.884
.063	.305	14.9	72.1	1.548801	.893
.073	.340	17.3	80.4	1.548840	.900
.088	.360	20.8	85.1	1.549003	.930
.140	.480	33.1	113.5	1.549164	.960
.220	.730	52.0	172.6	1.549270	.980

Table C-14. Jitter Data for Test 12

Sheet 1 of 1

E_o RMS (Volts)	E_o Peak-Peak (Volts)	Jitter RMS (Degrees)	Jitter Peak-Peak (Degrees)	T1 (Mbps)	ρ
.041	.260	9.7	61.5	1.54420	.298
.046	.275	10.9	65.0	1.54415	.308
.050	.285	11.8	67.4	1.54410	.317
.081	.350	19.1	82.7	1.54405	.326
.116	.460	27.4	108.7	1.54400	.336
.062	.310	14.7	73.3	1.54395	.345
.044	.265	10.4	62.6	1.54390	.354
.047	.255	11.1	60.3	1.54385	.363
.030	.220	7.1	52	1.54381	.371

Table C-15. Jitter Data for Test 13

Sheet 1 of 1

T1S (MHz)	Bandwidth (Hz)	BPO	Sequence Length (Bits)	Interval Length (Bits)	BER (Bits)	Total Error Count (Bits)
1.5458	1528	288	2^6	10^6	1.3×10^{-4}	136
	764				None	0
	382					
	191					
	96					
1.544935	764	576			2.6×10^{-3}	7565
	382				None	0
	191					
	96					
	48					

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